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Spartan-7 FPGA Board

T0006 · XC7S25 / XC7S50

DS#T0006 REV 2026/11/27 | PDF version | HTML version

Small form factor FPGA module with AMD Spartan-7

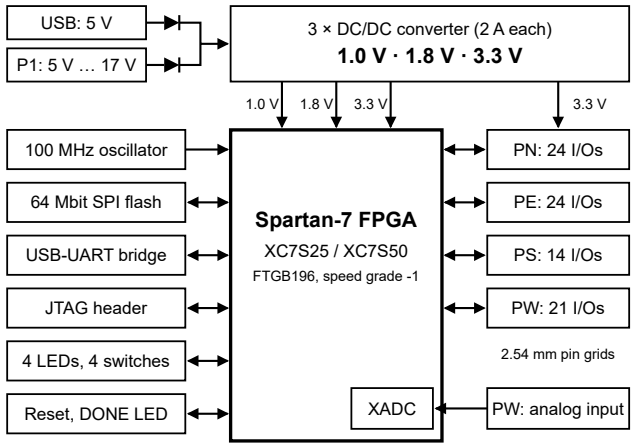
Features

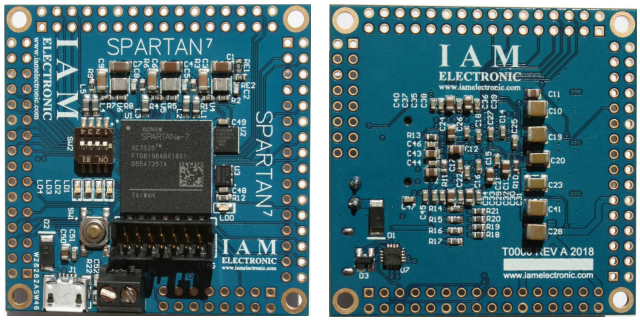
- AMD (Xilinx) Spartan-7 FPGA: XC7S25 or XC7S50
- Dimensions of 2″ × 2″ (50.8 mm × 50.8 mm)
- 83 user inputs/outputs (3.3 V), usable as up to 39 differential pairs
- 1 differential analog input (12 bit, 1 MSPS)
- 4 user LEDs
- 4 user switches
- USB-UART bridge with up to 3 Mbaud
- Powered via USB or external voltage supply from 5 V to 17 V
- 100 MHz on-board clock (±10 ppm)
- 64 Mbit configuration memory
- Standard JTAG header (14 pin)
- Out-of-the-box functionality, no mother- or carrier board required

Applications

- Industrial measurements and control
- Digital signal processing
- Interface adaptation
- Soft processor systems (MicroBlaze, RISC-V)
- Easy prototyping
- Education and research with FPGAs

Block diagram





Top side Bottom side

The photos show a board of REV A with XC7S25. By default, the board is **not** populated with pin headers on the 2.54 mm grid.

1. Description

The **small form factor Spartan-7 FPGA board** is an out-of-the-box FPGA module with dimensions of only 2″ × 2″ (50.8 mm × 50.8 mm). It is ready for use by simply connecting a power supply and programming the FPGA or the 64 Mbit SPI flash via the standard JTAG connector. The board operates with a USB power supply or an external power supply at the screw terminal P1 or at the pin grid. It supports a wide input voltage range from 5 V up to 17 V DC and provides 83 general purpose I/Os (GPIOs) on easily accessible pin grids at the edges of the board. Additionally there is a dedicated input for analog-to-digital conversion with a sample rate of up to 1 MSPS and a resolution of 12 bit (XADC of the FPGA). The on-board USB-UART bridge allows communication with a host at data rates of up to 3 Mbaud. Four programmable blue LEDs and four micro switches are available for user interaction. The board includes a stable 100 MHz clock source for the FPGA, which can also be clocked from external sources via the pin grids. The board is available with the XC7S25 and with the pin-compatible, larger XC7S50. It offers all basic functions for many FPGA applications on a tiny footprint without the need for an additional carrier board.

This data sheet describes boards of **REV B (2019)**. Typical characteristics measured on the board – die temperature, supply voltages under load, soft processor performance and USB-UART throughput – are given in section 6.

2. Variants

The board is assembled with one of two Spartan-7 devices in the FTGB196 package (speed grade -1, commercial temperature grade). Both devices have identical pin functions, so the pin-out, the constraint file and all tables of this data sheet are valid for both variants. The bitstreams are not interchangeable.

Tab. 1: FPGA resources of the two assembly variants (AMD DS180, UG470).

Resource	XC7S25-1FTGB196C	XC7S50-1FTGB196C
Logic cells	23,360	52,160
6-input LUTs / flip-flops	14,600 / 29,200	32,600 / 65,200
Slices	3,650	8,150
Distributed RAM (max.)	313 Kb	600 Kb
Block RAM (36 Kb blocks / total)	45 / 1,620 Kb	75 / 2,700 Kb
DSP slices (DSP48E1)	80	120
Clock management tiles (1 MMCM + 1 PLL each)	3	5
Analog-to-digital converter (XADC)	1	1
User I/Os on the pin grids / used on the board	83 / 17	83 / 17
Bitstream length (uncompressed)	9,934,432 bit	17,536,096 bit
Uncompressed bitstreams that fit into the 64 Mbit flash	6	3
JTAG IDCODE (without revision bits)	0x37C4093	0x362F093

3. Application information

3.1 Powering the board

The board can be powered via the USB connector J1 (Micro-USB) or with a voltage of 5 V to 17 V at the screw terminal P1. Each of the two inputs has a Schottky diode in series (D1 at P1, D2 at USB). Behind the diodes both inputs are connected to the common supply node VIN, from which three DC/DC converters generate the supply voltages of the board: 1.0 V (FPGA core), 1.8 V (FPGA auxiliary supply) and 3.3 V (I/O banks, on-board devices and the 3.3 V pins of the pin grids). The converters start one after the other in this order.

It is not recommended to use both power supply inputs simultaneously! If possible, the USB power supply by a host should be deactivated when using the screw terminal for powering the board. With sufficient caution, however, both inputs can be used in parallel: the diodes prevent a current from one source into the other, and the board is supplied from the higher of the two voltages. A test with 17 V input voltage and additional USB power supply showed no damage or impairments.

> **Make sure that the power supply is connected with the correct polarity!** Apart from the series diode at P1 the board has no input protection (no fuse, no over-voltage protection). The VIN pins of the pin grids are connected behind the diodes and are not protected at all. Fig. 1 shows the correct polarity of P1.

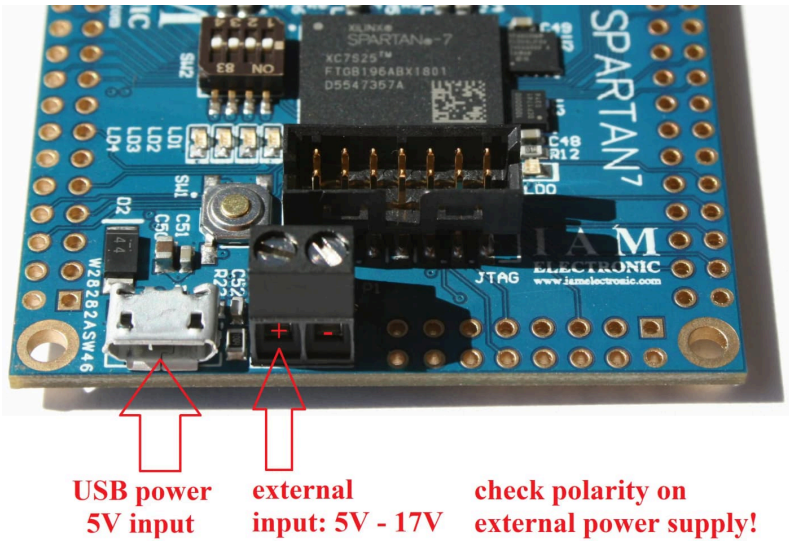


Fig. 1: Take care of the right polarity of the screw terminal power input P1. The positive terminal is located left.

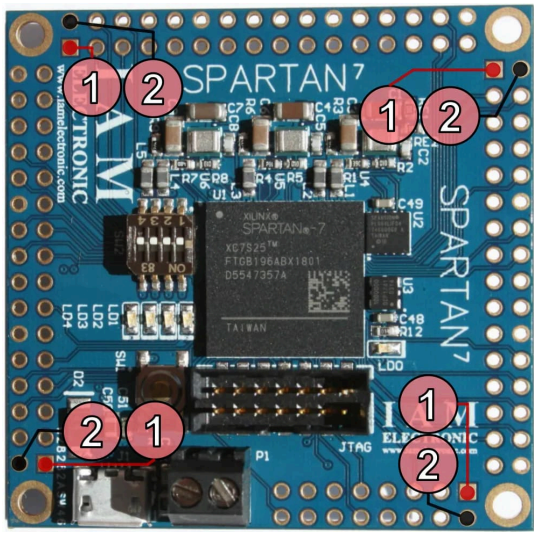


Fig. 2: Pin 1 of each pin grid (square pad) is VIN, pin 2 is the corresponding ground (GND).

Another way to power the board is to use the dedicated pins of the pin grids (see Fig. 2). Pin 1 of each grid (square pad) is connected to VIN, the corresponding ground (GND) is pin 2. The main purpose of these pins is to supply further modules or other devices, i.e. they are intended as a voltage *output*: with a power supply via the USB connector the voltage at pin 1 is approx. 4.7 V (USB voltage minus the forward voltage of the diode), with an external supply at P1 it is that voltage minus approx. 0.3 V. It is also possible to supply the FPGA board itself via these pins with 5 V to 17 V, but this should not be the preferred usage.

Without external loads a USB port is sufficient: the calculated supply current is about 60 mA for a small design and about 0.35 A for the highest load of the full-load test in section 6.2, which ran from a USB port (see Tab. 4). Loads connected to the 3.3 V or VIN pins must be added.

3.2 Programming the board

Both FPGA variants are supported by the free edition of the AMD Vivado Design Suite (Vivado Standard, formerly WebPACK; the XC7S25 since version 2018.1). A design is synthesized and downloaded to the FPGA with this toolchain. For this purpose, we recommend a supported programming cable like the Xilinx Platform Cable USB or the JTAG-HS3 programming cable from Digilent. The cable must fit the standard JTAG header with 14 pins (2 mm pitch). Some examples are shown in Fig. 3.

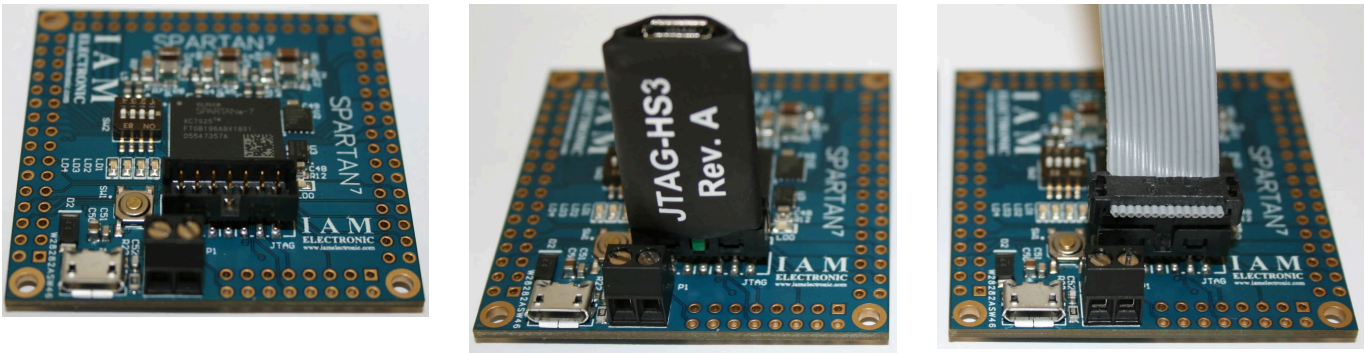


Fig. 3: On-board standard JTAG header (left) with plugged Digilent JTAG-HS3 programming cable (middle) or Xilinx Platform Cable USB (right).

There are several ways to program the FPGA. In the simplest case the Hardware Manager of Vivado programs the FPGA directly with a bit file (volatile). For a non-volatile configuration a configuration file has to be programmed into the on-board SPI flash. The configuration memory is an S25FL064L (Infineon, formerly Cypress). In the Hardware Manager choose the memory part `s25fl064l-spi-x1_x2_x4` (see Fig. 4); this part is supported since Vivado 2017.3.

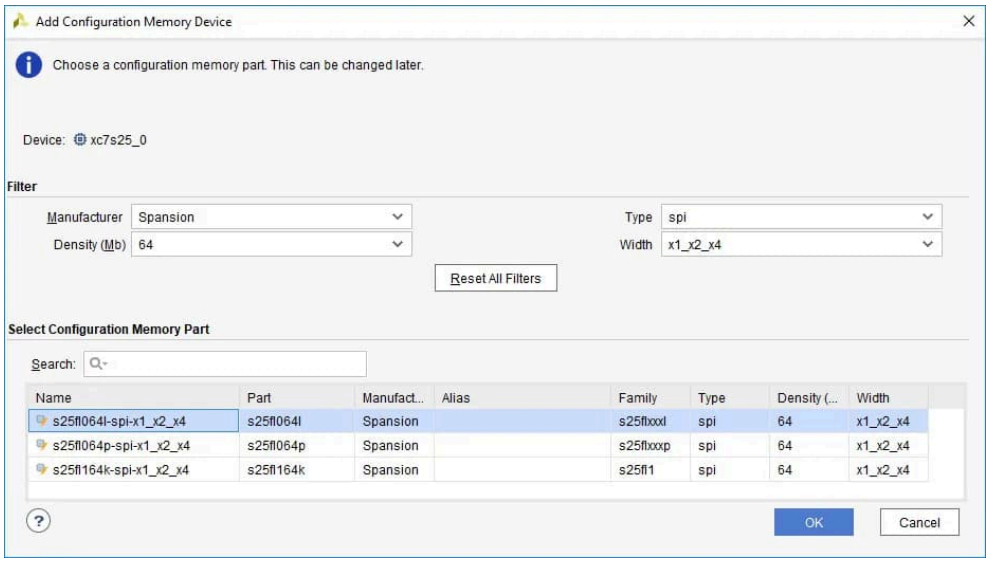


Fig. 4: Choose the right configuration memory part in Vivado.

Proper function of the device can be checked by reading the XADC values (internal supply voltages, die temperature), see Fig. 5.

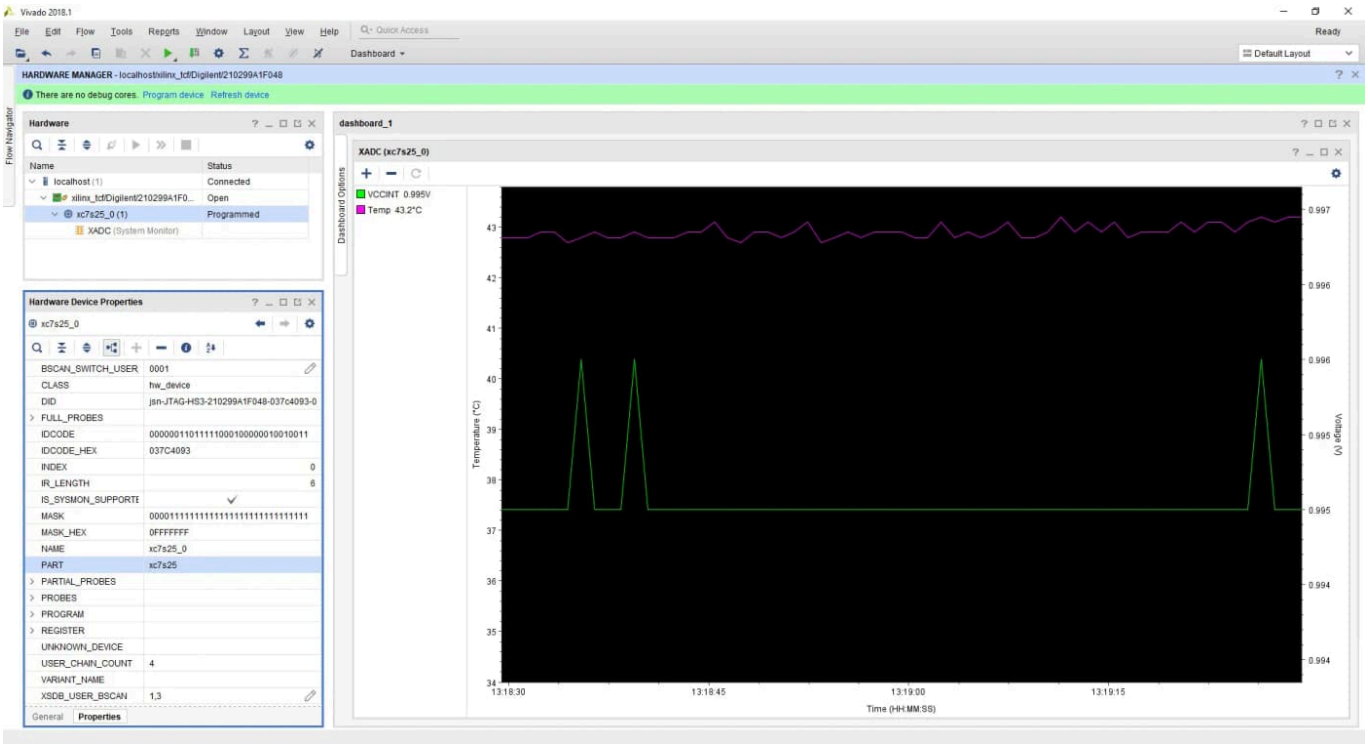


Fig. 5: The Vivado Hardware Manager reads the internal XADC values of the FPGA.

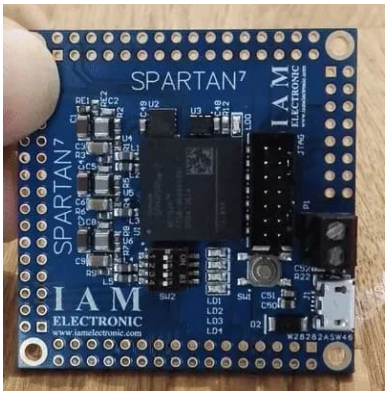


Fig. 6: "Hello world" reference design with blinking LEDs.

A "hello world" reference design for Vivado (blinking LEDs, see Fig. 6) is available at GitHub: github.com/iamelectronic/T0006_Spartan_7_Hello_World. After the design has been loaded, the four user LEDs start to blink.

3.3 Design constraints

All I/O banks of the FPGA (bank 0, 14 and 34) are powered with 3.3 V. We recommend the following constraints for the configuration of the FPGA and, for the fastest configuration from the SPI flash, the four-bit SPI mode:

```
set_property CFGBVS VCCO                       [current_design]
set_property CONFIG_VOLTAGE 3.3                [current_design]
set_property BITSTREAM.CONFIG.SPI_BUSWIDTH 4 [current_design]
set_property CONFIG_MODE SPIx4                 [current_design]
```

For single-ended I/Os use the I/O standard LVCMOS33 (or LVTTL), for differential outputs the Transition Minimized Differential Signaling (TMDS) standard:

```
set_property IOSTANDARD LVCMOS33 [get_ports {...}]
set_property IOSTANDARD TMDS_33  [get_ports {...}]
```

LVDS outputs are not available in banks powered with 3.3 V. LVDS inputs (`LVDS_25`) can be used with an external 100 Ω termination (`DIFF_TERM` = FALSE) as long as the input voltages stay within the limits of Tab. 3.

A constraint file with all pins of the board (for both FPGA variants) is available for download: t0006_revB_v1.2.xdc. Its pin assignments are identical to template v1.1 for boards of REV B; version 1.2 adds the FPGA pin name of every pin as a comment.

4. Electrical data

4.1 Absolute maximum ratings

Stresses beyond these values may cause permanent damage to the board. Functional operation is only specified within the recommended operating conditions.

Tab. 2: Absolute maximum ratings.

Parameter	Min.	Max.	Unit
Supply voltage at P1 or at the VIN pins of the pin grids[1]	–	17	V
Voltage at the I/O pins of the pin grids (board powered)[2]	−0.4	3.85	V
Voltage at the I/O pins of the pin grids (board not powered)[2]	−0.4	0.55	V
Current through the clamp diodes of an I/O pin[2]	–	10	mA
Voltage at the analog input pins VP, VN (PW pin 3 and 4)[3]	−0.1	1.9	V
Junction temperature of the FPGA[2]	–	125	°C

[1] 17 V is the maximum recommended input voltage of the DC/DC converters; higher voltages were not tested. A reversed voltage at the VIN pins can destroy the board. [2] Limits of the FPGA (AMD DS189): V_{CCO} + 0.55 V with V_{CCO} = 3.3 V. [3] Limit of the XADC (AMD UG480). The analog inputs are connected directly to the FPGA and are **not** 3.3 V tolerant.

4.2 Recommended operating conditions

Tab. 3: Recommended operating conditions.

Parameter	Min.	Typ.	Max.	Unit
External supply voltage at P1	5	–	17	V
Supply voltage at the USB connector J1	–	5	–	V
Input voltage at the I/O pins (LVCMOS33, LVTTL)	−0.2	–	3.5	V
Differential input voltage at the analog input (VP − VN), unipolar mode	0	–	1.0	V
Differential input voltage at the analog input (VP − VN), bipolar mode	−0.5	–	0.5	V
Output current of the 3.3 V converter (FPGA, on-board devices and external loads)[1]	–	–	2	A
Junction temperature of the FPGA (commercial grade)	0	–	85	°C

[1] The loads at the 3.3 V pins of the pin grids share this current with the FPGA and the on-board devices. With USB supply the available power is limited by the USB port. The permissible ambient temperature depends on the power dissipation of the FPGA design, see section 6.3; the other integrated circuits of the board (DC/DC converters, oscillator, USB-UART bridge, flash) are specified for at least −40 °C to +85 °C.

4.3 Electrical characteristics

Tab. 4: Electrical characteristics at an ambient temperature of 22 °C (typical values of one board, not guaranteed).

Parameter	Condition	Typ.	Unit
FPGA core voltage V_{CCINT} at the FPGA[1]	without load	1.003	V
Decrease of V_{CCINT} with the core current[1]	0 to 1.1 A	41.5	mV/A
Block RAM voltage V_{CCBRAM} at the FPGA[1]		1.004	V
Auxiliary voltage V_{CCAUX} at the FPGA[1]		1.789	V
I/O voltage V_{CCO}, voltage at the 3.3 V pins[2]	without load	3.27	V
Output current of each DC/DC converter (1.0 V, 1.8 V, 3.3 V)	maximum	2	A
Voltage at the VIN pins[2]	USB supply	4.7	V
Supply current[2]	5 V, FPGA configured, small design	60	mA
Additional supply current per watt of FPGA core power[2]	5 V / 12 V supply	250 / 110	mA/W
Clock frequency (U3)		100	MHz
Frequency stability of the clock[3]	−40 to +85 °C	±10	ppm
Period jitter of the clock[3]	RMS	3	ps
Baud rate of the USB-UART bridge[3]	range	300 to 3,000,000	baud
Data rate of the USB-UART bridge without loss[4]	one direction / both directions at the same time	300,000 / 240,000	bytes/s
Series resistor of the user LEDs / pull-up of the switches		100 / 4700	Ω

[1] Measured with the XADC of the FPGA (on-chip reference; accuracy of the supply sensors ±1 % plus ±1 % for the reference); the core current is the estimate of the Vivado power report, see section 6.4. [2] Calculated from the circuit and the data sheets of the components, not measured. [3] Data sheet values of the components (Microchip DSC1101, Silicon Labs CP2102N). [4] Measured, see section 6.6.

5. Pin description

The circuit diagram of the board is available as PDF: T0006 Spartan-7 FPGA board schematics. Fig. 7 gives an overview of the building blocks, which are described in the following sections.

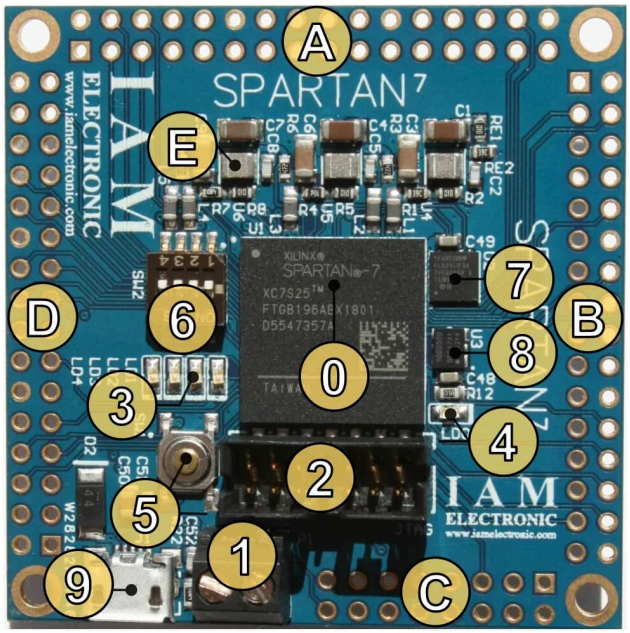


Fig. 7: Overview of all building blocks of the Spartan-7 FPGA board.

0 FPGA

The board is assembled with an AMD Spartan-7 FPGA XC7S25-1FTGB196C or XC7S50-1FTGB196C (see section 2). The speed grade of both devices is -1 and the junction temperature range is 0 °C to 85 °C (commercial grade). Other assemblies are available on request (see Ordering information). A master constraint file (see section 3.3) and a reference project for Vivado are available.

1 P1 screw terminal

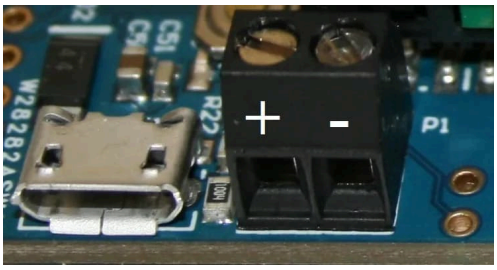


Fig. 8: Screw terminal P1 for power input (front view). The left terminal is positive, the right one is negative (GND).

The screw terminal P1 is for direct power supply with loose cables. The recommended wire range is 16 to 28 AWG, the wire strip length should be 3 to 4 mm. The circuitry is designed for an input voltage of 5 V to 17 V.

Make sure the polarity is correct when connecting the cables!

2 JTAG header

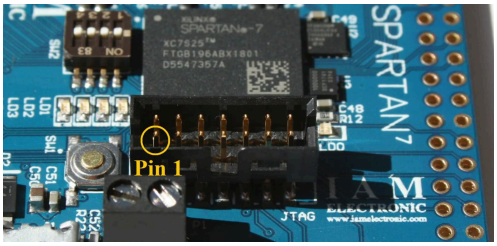


Fig. 9: Standard JTAG header, dual row with 14 pins (2.00 mm pitch).

The pin assignment of the JTAG header matches the 14-pin connectors of common programming cables. Some examples are shown in section 3.2.

Tab. 5: Pin-out of the JTAG header. All odd pins are connected to GND.

Pin	Signal	FPGA pin name	Bank	Ball
2	3.3 V (reference voltage for the cable)			
4	TMS	`TMS_0`	0	M6
6	TCK	`TCK_0`	0	A7
8	TDO	`TDO_0`	0	P6
10	TDI	`TDI_0`	0	P7
12, 14	not connected			

3 User LEDs (blue)

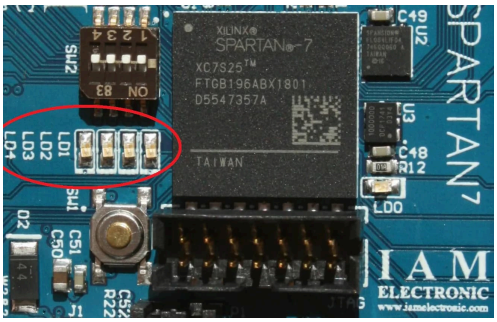


Fig. 10: User LEDs (blue) LD1, LD2, LD3 and LD4.

Next to the FPGA there is a row of four blue LEDs with the designators LD1, LD2, LD3 and LD4. The output drivers of the FPGA pins power the LEDs directly through a 100 Ω series resistor.

Tab. 6: Pin assignment of the user LEDs.

Board pin	Note	FPGA pin name	Bank	Ball
LD1	High = LED on	`IO_L18P_T2_34`	34	M1
LD2	High = LED on	`IO_25_14`	14	M10
LD3	High = LED on	`IO_0_34`	34	B6
LD4	High = LED on	`IO_L18N_T2_34`	34	L1

4 Configuration LED

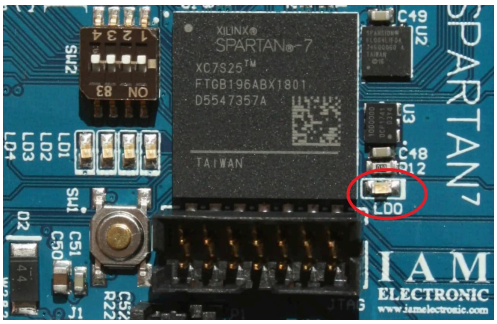


Fig. 11: Configuration LED LD0.

LD0 indicates the completion of the configuration sequence. Until the FPGA is configured the LED is off; in normal operation LD0 is permanently switched on.

Tab. 7: Assignment of the configuration LED.

Board pin	Note	FPGA pin name	Bank	Ball
LD0	Configuration done = LED on	`DONE_0`	0	P9

5 Reset button

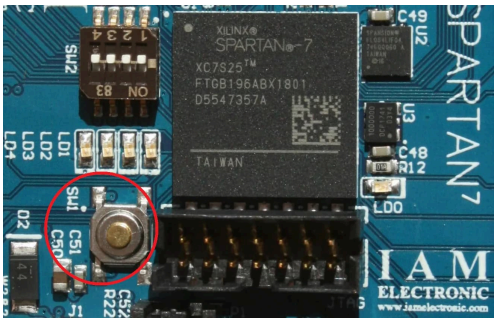


Fig. 12: Reset button SW1.

The button SW1 next to the JTAG connector triggers a manual reset (reconfiguration) of the FPGA. In the unpressed state the PROGRAM_B pin of the FPGA is pulled high; while the button is pushed, the pin is tied to GND. On the falling edge the configuration of the FPGA is cleared, and a new configuration sequence starts with the following rising edge. Because the FPGA is permanently set to Master SPI mode, the configuration is then loaded from the SPI flash.

Tab. 8: Assignment of the reset button SW1.

Board pin	Note	FPGA pin name	Bank	Ball
SW1	Unpressed = high, pressed = low	PROGRAM_B_0	0	L7

6 Micro switches

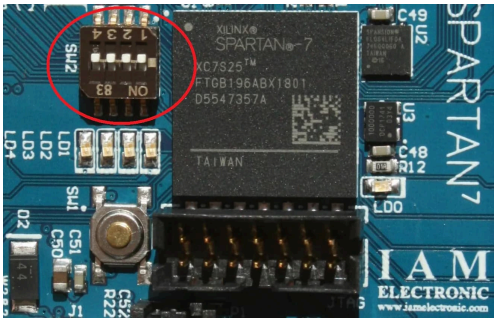


Fig. 13: Micro DIP switches SW2.

The four micro DIP switches SW2 can be used for user inputs. Due to their small dimensions they are best suited for coding fixed values or states. In the OFF state of a switch the associated FPGA pin is pulled high (4.7 kΩ), in the ON state it is tied to GND. The ON position is marked on the case.

Tab. 9: Assignment of the micro switches SW2.

Board pin	Note	FPGA pin name	Bank	Ball
SW2 No. 1	Off = high, on = low	IO_L17P_T2_34	34	J4
SW2 No. 2	Off = high, on = low	IO_L17N_T2_34	34	J3
SW2 No. 3	Off = high, on = low	IO_L16P_T2_34	34	K4
SW2 No. 4	Off = high, on = low	IO_L16N_T2_34	34	K3

7 Configuration memory (SPI flash)

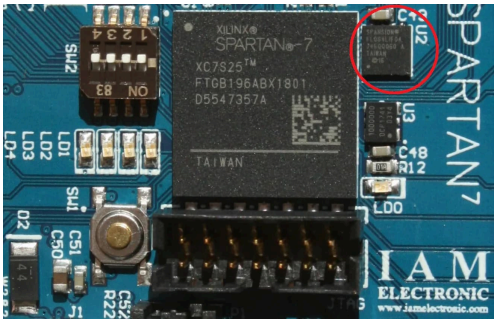


Fig. 14: 64 Mbit SPI configuration flash U2.

The non-volatile configuration of the FPGA is loaded in Master SPI mode (mode pins M[2:0] = 001) from the memory device U2, an S25FL064L with 64 Mbit. In Vivado choose the device `s25fl064l-spi-x1_x2_x4` (supported since Vivado 2017.3, see section 3.2). The length of an uncompressed bitstream is 9,934,432 bit for the XC7S25 and 17,536,096 bit for the XC7S50 (AMD UG470), so the memory can hold several configurations or additional user data.

During configuration all I/O pins are in high impedance without pull-up resistors, because the pin PUDC_B is permanently pulled high.

Tab. 10: Assignment of the SPI flash and of the configuration pins.

Board pin	Note	FPGA pin name	Bank	Ball
U2 pin 6	SCK	CCLK_0	0	A8
U2 pin 1	CS#	IO_L6P_T0_FCS_B_14	14	C11
U2 pin 5	SI / IO0	IO_L1P_T0_D00_MOSI_14	14	B11
U2 pin 2	SO / IO1	IO_L1N_T0_D01_DIN_14	14	B12
U2 pin 3	WP# / IO2	IO_L2P_T0_D02_14	14	D10
U2 pin 7	HOLD# / IO3	IO_L2N_T0_D03_14	14	C10
Pull-up R13	High	M0_0	0	M7
GND	Low	M1_0	0	M8
GND	Low	M2_0	0	M9
Pull-up R10	High	IO_L3P_T0_DQS_PUDC_B_14	14	B10

8 Clock source 100 MHz

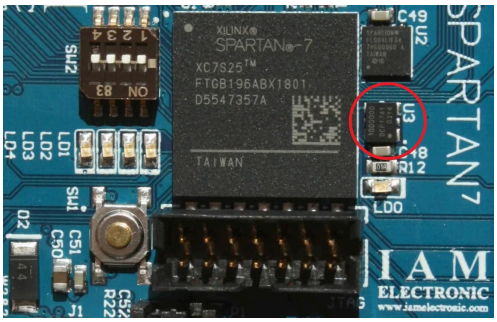


Fig. 15: 100 MHz clock source U3.

A low-jitter MEMS oscillator generates a stable system clock for the FPGA: the DSC1101CI5-100.0000 (U3) from Microchip with an output frequency of 100 MHz and a frequency stability of ±10 ppm from −40 °C to 85 °C. The clock source has a single-ended CMOS output (high: min. 2.97 V, low: max. 0.33 V), which is routed directly to a multi-region clock capable (MRCC) input in bank 14.

Tab. 11: Assignment of the clock signal.

Board pin	Note	FPGA pin name	Bank	Ball
U3 pin 4	100 MHz output of U3	`IO_L13P_T2_MRCC_14`	14	H11

On boards of REV A (2018) the oscillator is connected to H12 (IO_L13N_T2_MRCC_14) and PE pin 18 to H11.

9 USB-UART bridge

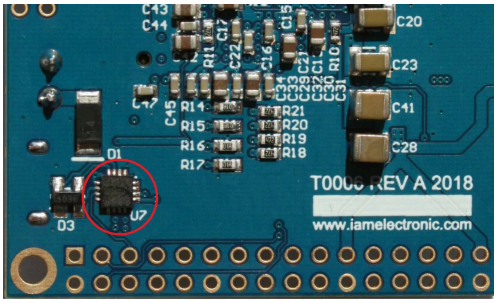


Fig. 16: USB-UART bridge CP2102N (U7) on the bottom side.

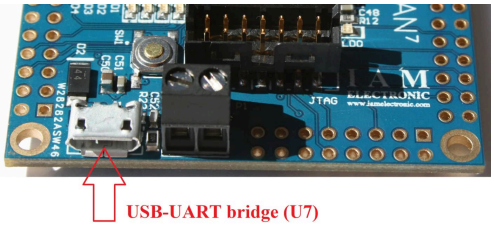


Fig. 17: USB connector J1 (Micro-USB).

The board includes a single-chip USB to UART bridge CP2102N-A01-GQFN20 from Silicon Labs (U7, on the bottom side of the board) for baud rates of up to 3 Mbaud. Please download the CP210x Virtual COM Port (VCP) drivers from silabs.com if your operating system does not install them automatically. After that the FPGA communicates with the host via a virtual COM port.

Only the data lines RXD and TXD are connected to the FPGA; there are no handshake lines. Measured data rates are given in section 6.6. The bridge is supplied from the 3.3 V rail of the board, so the virtual COM port is also available with an external supply as soon as the USB cable is plugged in; it stays available while the FPGA is configured via JTAG.

Tab. 12: Assignment of the USB-UART signals.

Board pin	Note	FPGA pin name	Bank	Ball
U7 pin 17	FPGA TXD → USB host RXD	`IO_L23N_T3_34`	34	M4
U7 pin 18	FPGA RXD ← USB host TXD	`IO_L23P_T3_34`	34	M5

A I/O grid PN (north, 32 pins)

The pin grid on the upper side of the board (north) has 32 pins with 2.54 mm pitch: 24 general purpose I/Os (GPIOs), three 3.3 V output pins, one VIN pin (see section 3.1) and four ground pins. All I/Os belong to banks powered with 3.3 V.

In the following tables the odd pins of a grid are listed on the left and the even pins on the right. Two pins with the names `LnP` and `LnN` of the same bank form a differential pair; in total the four grids provide 39 complete pairs. Pins marked with ^{C} are clock capable inputs (MRCC: multi-region, SRCC: single-region); 7 of the pairs are clock capable.

Tab. 13: Pin mapping of pin grid PN.

Pin	Ball	Bank	FPGA pin name / function	Pin	Ball	Bank	FPGA pin name / function
1			**VIN (supply)**	**2**			**GND**
3	D1	34	IO_L11P_T1_SRCC_34^{C}	**4**	C1	34	IO_L11N_T1_SRCC_34^{C}
5	B1	34	IO_L5N_T0_34	**6**	B2	34	IO_L5P_T0_34
7	D3	34	IO_L1P_T0_34	**8**	C3	34	IO_L1N_T0_34
9	A2	34	IO_L3N_T0_DQS_34	**10**	B3	34	IO_L3P_T0_DQS_34
11			**3.3 V (output)**	**12**			**GND**
13	A3	34	IO_L2N_T0_34	**14**	A4	34	IO_L2P_T0_34
15	B5	34	IO_L4P_T0_34	**16**	A5	34	IO_L4N_T0_34
17	C5	34	IO_L6P_T0_34	**18**	C4	34	IO_L6N_T0_VREF_34
19	E4	34	IO_L7P_T1_34	**20**	D4	34	IO_L7N_T1_34
21			**3.3 V (output)**	**22**			**GND**
23	A10	14	IO_L3N_T0_DQS_EMCCLK_14	**24**	C12	14	IO_L6N_T0_D08_VREF_14
25	A13	14	IO_L4N_T0_D05_14	**26**	A12	14	IO_L4P_T0_D04_14
27	D12	14	IO_L8P_T1_D11_14	**28**	D13	14	IO_L8N_T1_D12_14
29	B14	14	IO_L5N_T0_D07_14	**30**	B13	14	IO_L5P_T0_D06_14
31			**3.3 V (output)**	**32**			**GND**

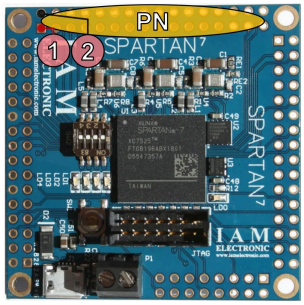


Fig. 18: Pin grid PN with 32 positions.

B I/O grid PE (east, 32 pins)

The pin grid on the right side of the board (east) has 32 pins with 2.54 mm pitch: 24 general purpose I/Os (GPIOs), three 3.3 V output pins, one VIN pin and four ground pins. All I/Os belong to bank 14, which is powered with 3.3 V. Some pins of bank 14 have a second function during the configuration of the FPGA (D00 to D31, EMCCLK, CSI_B, DOUT, RDWR_B). On this board the FPGA is configured from the SPI flash, so these pins are free for the user design after configuration.

Tab. 14: Pin mapping of pin grid PE.

Pin	Ball	Bank	FPGA pin name / function	Pin	Ball	Bank	FPGA pin name / function
1			**VIN (supply)**	**2**			**GND**
3	C14	14	IO_L11N_T1_SRCC_14^{C}	**4**	D14	14	IO_L11P_T1_SRCC_14^{C}
5	F12	14	IO_L7P_T1_D09_14	**6**	E12	14	IO_L7N_T1_D10_14
7	F11	14	IO_L12N_T1_MRCC_14^{C}	**8**	G11	14	IO_L12P_T1_MRCC_14^{C}
9	F13	14	IO_L10P_T1_D14_14	**10**	E13	14	IO_L10N_T1_D15_14
11			**3.3 V (output)**	**12**			**GND**
13	G14	14	IO_L9P_T1_DQS_14	**14**	F14	14	IO_L9N_T1_DQS_D13_14
15	H13	14	IO_L14P_T2_SRCC_14^{C}	**16**	H14	14	IO_L14N_T2_SRCC_14^{C}
17	E11	14	IO_0_14	**18**	H12	14	IO_L13N_T2_MRCC_14^{C}
19	J11	14	IO_L17P_T2_D30_14	**20**	J12	14	IO_L17N_T2_D29_14
21			**3.3 V (output)**	**22**			**GND**
23	J13	14	IO_L18P_T2_D28_14	**24**	J14	14	IO_L18N_T2_D27_14
25	M13	14	IO_L15P_T2_DQS_RDWR_B_14	**26**	L14	14	IO_L15N_T2_DQS_DOUT_CSO_B_14
27	L12	14	IO_L16P_T2_CSI_B_14	**28**	L13	14	IO_L16N_T2_D31_14
29	N14	14	IO_L21P_T3_DQS_14	**30**	M14	14	IO_L21N_T3_DQS_D22_14
31			**3.3 V (output)**	**32**			**GND**

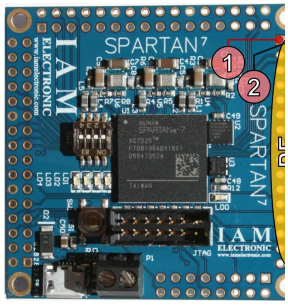


Fig. 19: Pin grid PE with 3 positions.

C I/O grid PS (south, 16 pins)

The pin grid on the lower side of the board (south) has 16 pins with 2.54 mm pitch: 14 general purpose I/Os (GPIOs), one VIN pin and one ground pin. All I/Os belong to banks powered with 3.3 V.

Tab. 15: Pin mapping of pin grid PS.

Pin	Ball	Bank	FPGA pin name / function	Pin	Ball	Bank	FPGA pin name / function
1			**VIN (supply)**	**2**			**GND**
3	M12	14	IO_L20N_T3_D23_14	**4**	M11	14	IO_L20P_T3_D24_14
5	P13	14	IO_L22N_T3_D20_14	**6**	P12	14	IO_L22P_T3_D21_14
7	N11	14	IO_L23N_T3_D18_14	**8**	N10	14	IO_L23P_T3_D19_14
9	P11	14	IO_L24N_T3_D16_14	**10**	P10	14	IO_L24P_T3_D17_14
11	K11	14	IO_L19P_T3_D26_14	**12**	K12	14	IO_L19N_T3_D25_VREF_14
13	P5	34	IO_L24P_T3_34	**14**	N4	34	IO_L24N_T3_34
15	L5	34	IO_25_34	**16**	P4	34	IO_L21P_T3_DQS_34

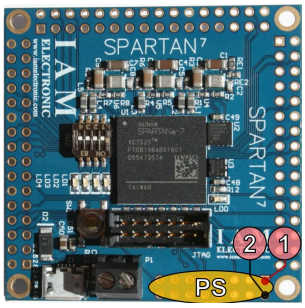


Fig. 20: Pin grid PS with 16 positions.

D I/O grid PW (west, 32 pins)

The pin grid on the left side of the board (west) has 32 pins with 2.54 mm pitch: 21 general purpose I/Os (GPIOs), one differential analog input, one status pin, three 3.3 V output pins, one VIN pin and four ground pins. All I/Os belong to bank 34, which is powered with 3.3 V.

Analog input (pin 3 and 4): the pins are connected directly to the dedicated XADC input VP/VN of the FPGA, without filter or protection. The input range is 0 V to 1 V (unipolar) or ±0.5 V (bipolar); the pins are not 3.3 V tolerant (Tab. 2). An anti-aliasing filter with at least 100 Ω in series is recommended.

PG3V3 (pin 5): power-good signal of the 3.3 V converter (open drain with 4.7 kΩ pull-up to 3.3 V; high: the supply voltages are stable). The signal is also connected to the INIT_B pin of the FPGA and to the reset input of the USB-UART bridge. It must not be driven high by an external circuit.

Tab. 16: Pin mapping of pin grid PW.

Pin	Ball	Bank	FPGA pin name / function	Pin	Ball	Bank	FPGA pin name / function
1			**VIN (supply)**	**2**			**GND**
3	G8	0	VP_0 (analog input, positive)	**4**	H7	0	VN_0 (analog input, negative)
5			**PG3V3 (power good)**	**6**	P3	34	IO_L21N_T3_DQS_34
7	P2	34	IO_L20P_T3_34	**8**	N1	34	IO_L20N_T3_34
9	M2	34	IO_L19N_T3_VREF_34	**10**	M3	34	IO_L19P_T3_34
11			**3.3 V (output)**	**12**			**GND**
13	L2	34	IO_L22N_T3_34	**14**	L3	34	IO_L22P_T3_34
15	H4	34	IO_L13P_T2_MRCC_34^{C}	**16**	H3	34	IO_L13N_T2_MRCC_34^{C}
17	J2	34	IO_L15P_T2_DQS_34	**18**	J1	34	IO_L15N_T2_DQS_34
19	H2	34	IO_L14P_T2_SRCC_34^{C}	**20**	H1	34	IO_L14N_T2_SRCC_34^{C}
21			**3.3 V (output)**	**22**			**GND**
23	F1	34	IO_L9N_T1_DQS_34	**24**	G1	34	IO_L9P_T1_DQS_34
25	F3	34	IO_L8P_T1_34	**26**	F2	34	IO_L8N_T1_34
27	G4	34	IO_L12P_T1_MRCC_34^{C}	**28**	F4	34	IO_L12N_T1_MRCC_34^{C}
29	E2	34	IO_L10P_T1_34	**30**	D2	34	IO_L10N_T1_34
31			**3.3 V (output)**	**32**			**GND**

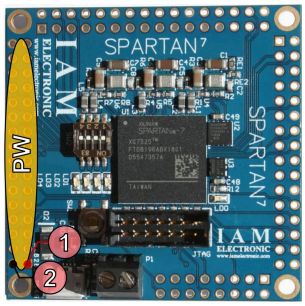


Fig. 21: Pin grid PW with 32 positions.

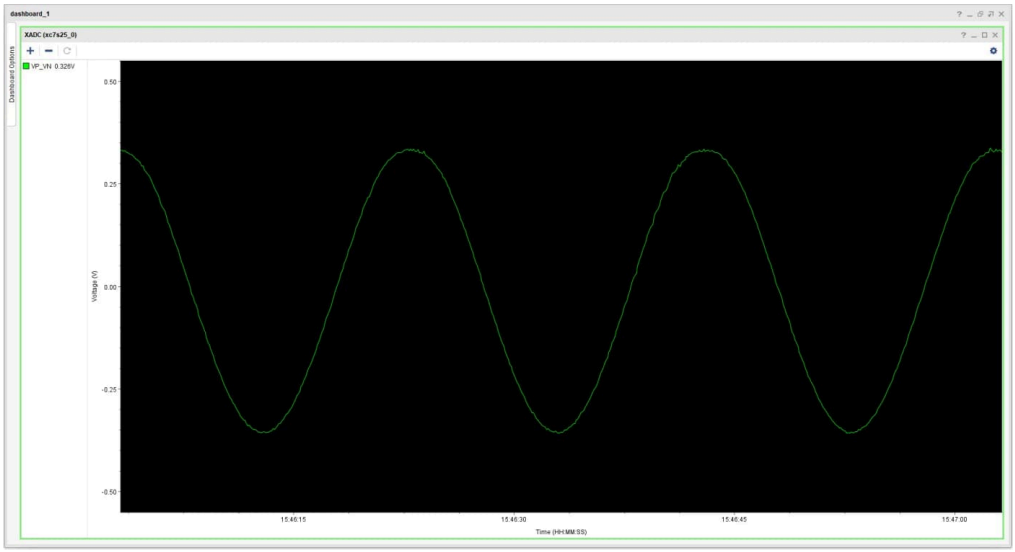


Fig. 22: Example of using the analog input of the FPGA. The Vivado Hardware Manager can be used to visualize the samples of the analog input.

E DC/DC converters

Three step-down converter modules (TPS82140) generate the supply voltages of the FPGA from VIN; each of them can deliver up to 2 A. The 3.3 V converter supplies the I/O banks of the FPGA (bank 0, 14 and 34), the on-board devices and the 3.3 V pins of the pin grids. The current of all loads connected to the board and of the FPGA itself must not exceed 2 A in total. The 1.0 V and 1.8 V rails are not available at the pin grids. Measured voltages at the FPGA are given in section 6.4.

6. Typical characteristics

6.1 Test conditions

Unless otherwise noted: one board T0006 REV B with XC7S50-1FTGB196C, supplied from a USB port, in still air without heat sink or forced cooling at an ambient temperature of approx. 22 °C. Designs were built with Vivado 2025.1. Die temperature and supply voltages were measured with the XADC of the FPGA (on-chip reference, 256 samples averaged; sensor accuracy according to AMD DS189: temperature ±4 °C, supply voltages ±1 %, plus ±1 % for the reference). The power dissipation and the core current of the FPGA were **not** measured; the values are the estimates of the Vivado power report for each operating point. All values are typical values of a single board and are not guaranteed.

6.2 Full-load test

The full-load test design fills the XC7S50 almost completely: 30,831 LUTs (94.6 %), 62,483 flip-flops (95.8 %), all 8,150 slices, all 75 block RAMs, all 120 DSP slices and all MMCMs and PLLs. The load logic is clocked with 195 MHz and checks itself at speed. The power dissipation is set with the toggle rate: at a toggle rate of 1/8 every flip-flop and every LUT output of the load logic changes its state in one of eight clock cycles, every block RAM is written and read in one of eight clock cycles, and the DSP slices get new operands in one of eight clock cycles. A toggle rate of 1/8 (12.5 %) is the default assumption of the Vivado power analysis for a typical design. Tab. 17 shows the XADC readings at the end of each load step of 4 to 5 minutes. The self-check reported no error in any step, and the whole test ran from a USB port.

Tab. 17: Full-load test of the XC7S50 board at 195 MHz (ambient temperature 22 °C, USB supply, no heat sink).

Load	FPGA power[1] [W]	Core current[1] [A]	Die temperature [°C]	V_{CCINT} [V]	V_{CCBRAM} [V]	V_{CCAUX} [V]
FPGA configured, clock off	0.08	0.02	35.5	1.003	1.004	1.789
clock tree only	0.39	0.28	47.3	0.989	1.004	1.787
load logic, toggle rate 1/64[2]	0.49	0.38	49.0	0.986	1.004	1.788
load logic, toggle rate 1/32[2]	0.59	0.48	51.5	0.982	1.004	1.788
load logic, toggle rate 1/16[2]	0.79	0.68	56.8	0.974	1.003	1.788
load logic, toggle rate 3/32[2]	0.99	0.88	63.8	0.966	1.003	1.789
load logic, toggle rate 1/8[2]	1.20	1.09	71.2	0.957	1.003	1.790

[1] Vivado estimate for the operating point, not measured.
[2] Load logic: all LUT/flip-flop chains, all block RAMs and all DSP slices are active. The four additional MMCMs and the five PLLs are switched off in these steps; their influence is given in section 6.4.

Boards with XC7S25. The test was run with the XC7S50 because it is the worst case for the board: both variants use the same DC/DC converters, ferrite beads and PCB, and the XC7S50 contains more than twice the logic. The board passed this test without any error. For the same test design in the XC7S25 (89 % of the LUTs, 90 % of the flip-flops, all 45 block RAMs and all 80 DSP slices at 195 MHz and a toggle rate of 1/8) Vivado estimates 0.56 W and a core current of 0.46 A, less than half of the 1.20 W and 1.09 A of the XC7S50. A board with XC7S25 therefore has more margin for the core voltage than Tab. 17 shows. The XC7S25 itself was not measured.

6.3 Die temperature

The die temperature rises linearly with the power dissipation of the FPGA (Fig. 23). For the XC7S50 board without heat sink in still air the measurement gives

$$T_{die} \approx T_{ambient} + 12\ K + 31\ K/W \times P_{FPGA}$$

The offset of 12 K is the heating of the board by the DC/DC converters, the oscillator and the quiescent power of the FPGA; it also contains the tolerance of the temperature sensor. With the junction temperature limit of 85 °C (commercial grade) this results in a permissible power dissipation of about 1.7 W at 22 °C ambient temperature. Fig. 24 and Tab. 18 show the estimate for higher ambient temperatures (linear extrapolation of the measurement at 22 °C). Up to an ambient temperature of about 31 °C the core supply voltage, not the temperature, limits the usable power (section 6.4). Designs close to these limits should monitor the die temperature with the XADC. The XC7S25 variant was not measured; because of its smaller die a slightly higher thermal resistance is expected.

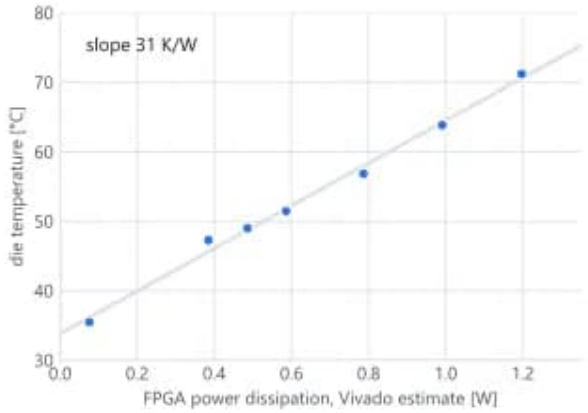


Fig. 23: Die temperature (XADC) against the estimated power dissipation of the FPGA at 22 °C ambient temperature.

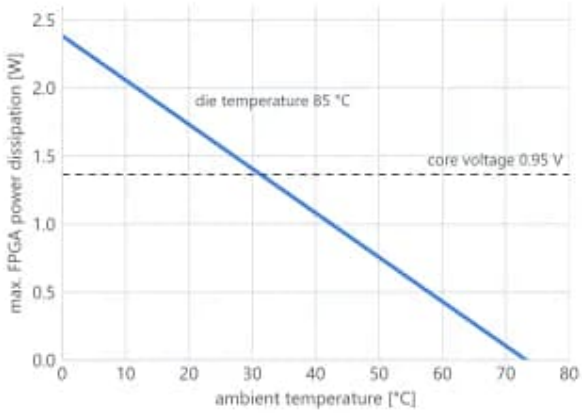


Fig. 24: Estimated permissible power dissipation of the FPGA against the ambient temperature.

Tab. 18: Estimated permissible power dissipation of the FPGA (XC7S50, no heat sink, still air).

Ambient temperature	Limit by the die temperature (85 °C)	Limit by the core voltage (0.95 V)
25 °C	1.6 W	1.4 W
40 °C	1.1 W	1.4 W
50 °C	0.8 W	1.4 W
60 °C	0.4 W	1.4 W

6.4 Supply voltages at the FPGA

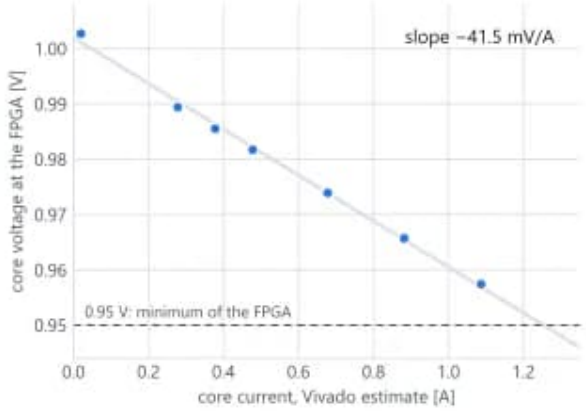


Fig. 25: Core voltage V_{CCINT} at the FPGA (XADC) against the estimated core current.

The DC/DC converter regulates the core voltage at its output. The ferrite bead between the converter and the FPGA (L1) causes a voltage drop that increases with the core current (Fig. 25):

$$V_{CCINT} \approx 1.002\ V - 41.5\ mV/A \times I_{CCINT}$$

The minimum core voltage of the FPGA (0.95 V) is reached at a core current of about 1.25 A, which corresponds to a power dissipation of about 1.4 W. The set point of the converter and the resistance of the ferrite bead (max. 50 mΩ) vary from board to board: designs with a core current of more than approx. 0.6 A should check V_{CCINT} with the XADC.

V_{CCBRAM} and V_{CCAUX} are almost independent of the load (Tab. 17). Running four MMCMs and five PLLs at the same time lowers V_{CCAUX} from 1.789 V to 1.768 V.

6.5 Soft processor performance

Both soft processors of the Vivado IP catalog, MicroBlaze and MicroBlaze V (RISC-V, RV32IMC), were implemented side by side in the XC7S50 and run the CoreMark and Dhrystone benchmarks from block RAM (64 KB per processor). Tab. 19 lists the results for the pipeline configurations of both processors. f_{max} is the limit of the static timing analysis (STA) for the complete processor system, i.e. the value for the worst case of speed grade -1; the scores at f_{max} are calculated from the measured scores per MHz (Fig. 26). On the tested board at room temperature all configurations ran the benchmark correctly far beyond the STA limit (up to 167 to 240 MHz, depending on the configuration); this margin is not guaranteed and must not be used in a design.

Tab. 19: MicroBlaze and MicroBlaze V in the XC7S50-1: clock frequency, benchmark results and resources of the processor core.

Processor	Pipeline	f_{max} [MHz]	CoreMark/MHz	CoreMark at f_{max}	DMIPS/MHz	DMIPS at f_{max}	LUTs	Flip-flops
MicroBlaze	3-stage (area)	139	1.82	253	0.99	138	1,145	609
MicroBlaze V	3-stage (area)	124	2.08	259	1.00	124	1,781	795
MicroBlaze V	4-stage (throughput)	101	2.74	276	1.54	155	2,636	1,379
MicroBlaze	5-stage (performance)	114	2.11	239	1.31	149	1,468	1,028
MicroBlaze V	5-stage (performance)	106	2.48	264	1.47	157	2,789	1,482
MicroBlaze	8-stage (frequency)	146	1.57	229	1.03	151	1,934	1,656
MicroBlaze V	8-stage (frequency)	100	1.72	172	0.80	80	3,520	2,872

CoreMark 1.0 (12 s run time, validated check sums) and Dhrystone 2.1, GCC 13.3 with -O2 (Dhrystone without inlining), code and data in block RAM. MicroBlaze with barrel shifter, 64-bit multiplier, divider and pattern comparator; MicroBlaze V as RV32IMC. Clock frequencies generated from the 100 MHz oscillator with an MMCM; LUTs and flip-flops of the processor core without memory and peripherals.

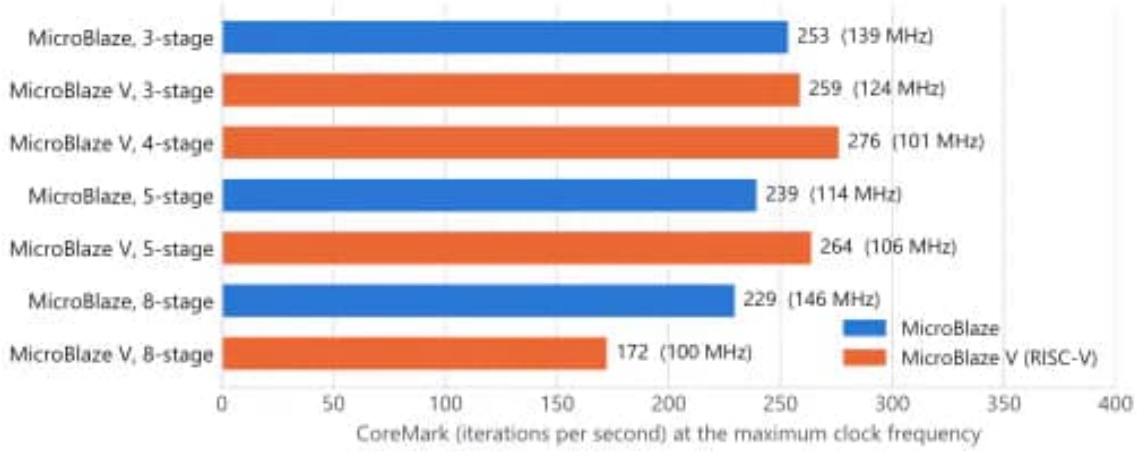


Fig. 26: CoreMark score at the maximum clock frequency of the static timing analysis.

6.6 USB-UART data rates

The USB-UART bridge was tested with three small FPGA designs: a loop-back (TXD follows RXD, so data flows in both directions at the same time), a data generator (FPGA to PC) and a receiver that returns a check sum for every 256 bytes (PC to FPGA). A Windows 10 PC (USB 3 root port, driver version 10.1.10) sent random data without pauses and checked every byte (Tab. 20).

Tab. 20: Error-free data transfer through the USB-UART bridge (8 data bits, no parity, 1 stop bit).

Transfer	Baud rate	Data volume	Data rate per direction	Result
One direction: FPGA → PC	3,000,000	18.0 MB	300,000 bytes/s	no error
One direction: PC → FPGA	3,000,000	6.0 MB	300,000 bytes/s	no error
Both directions at the same time	9,600 to 2,400,000 (10 rates)	25.2 MB	up to 240,000 bytes/s	no error
Both directions at the same time, data rate limited to 70 % of the line rate	3,000,000	12.6 MB	210,000 bytes/s	no error

The bridge transfers up to 300,000 bytes per second in one direction (3 Mbaud) and up to 240,000 bytes per second in both directions at the same time (2.4 Mbaud) without errors. Beyond that, simultaneous traffic in both directions overruns the bridge, because the board has no handshake lines: with continuous data at the full line rate in both directions, 4 % of the received bytes were lost at 2.67 Mbaud and 12 % at 3 Mbaud (no wrong bytes, the same result in 5 runs). At 3 Mbaud both directions can be used at the same time as long as the average data rate stays below about 70 % of the line rate, or with bursts of up to 1,024 bytes. The PC should start a 3 Mbaud data stream of the FPGA after it has opened the COM port – when the stream was already running while the port was opened, the reception stalled in some cases.

7. Mechanical data

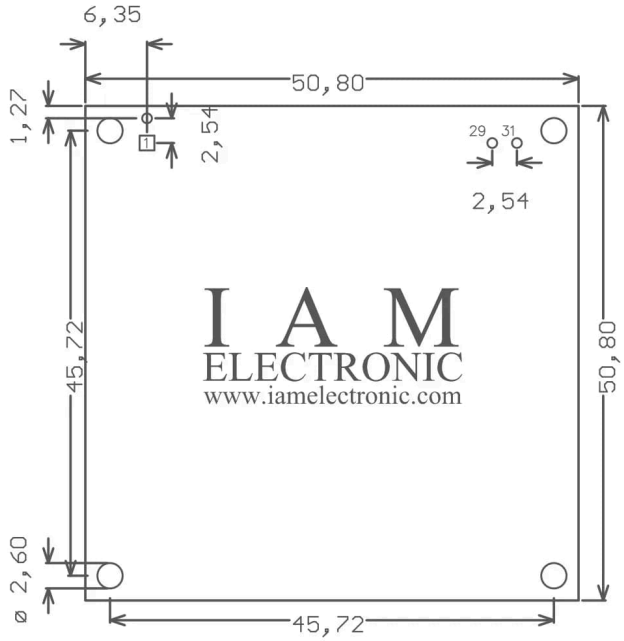


Fig. 27: Mechanical dimensions of the FPGA board (board outline and mounting holes). All dimensions are in millimeters.

Tab. 21: Mechanical data.

Parameter	Value
Board outline	50.8 mm × 50.8 mm (2″ × 2″)
Height (with JTAG header and screw terminal)	approx. 11.5 mm
Weight	approx. 15 g
Mounting holes	4 × Ø 2.6 mm, 45.72 mm × 45.72 mm
Pin grids	2.54 mm pitch, two rows; three grids with 32 pins, one with 16 pins
Suitable pin header (not included)	e.g. Samtec TSW-116-08-L-D-RA (32 pins, right angle)
JTAG header	2 × 7 pins, 2.00 mm pitch, shrouded
USB connector	Micro-USB, type B
Screw terminal P1	2 poles, wires 16 to 28 AWG

8. Ordering information

The T0006 Spartan-7 FPGA board can be ordered at various online market places, or you can request a quotation by sending an e-mail to info@iamelectronic.com.

Tab. 22: Assembly variants of the Spartan-7 FPGA board.

Product no.	Description	Market place	Standard lead time
T0006	Spartan-7 FPGA board with **XC7S25-1FTGB196C**	IAM ELECTRONIC shop eBay #184078435546 Tindie #13786	Currently out of stock
T0006 (XC7S50)	Spartan-7 FPGA board with **XC7S50-1FTGB196C**	Request a quote	On request

9. Document history

Document number: DS#T0006

Revision	Changes
2026/11/27	New layout and PDF version. Added: XC7S50 variant, electrical data, typical characteristics (full load, die temperature, supply voltages, soft processors, USB-UART), block diagram, pin details, constraint template v1.2. Corrected: three pin names, bitstream length, numbering. XC7S25 variant out of stock.
2021/09/17	Added link to schematics PDF file in section 3.
2021/07/09	Fixed pin locations of the 100 MHz clock input.
2019/12/18	Changed 100 MHz clock input pin for board REV B 2019, changed pin-out for PE pin 18 (all changes apply to board REV B 2019), added link to the master XDC file at GitHub.
2019/12/11	Fixed board pin names in the pin mapping of PW, updated ordering information.
2018/08/23	Added online market places in the ordering information.
2018/08/07	Initial release.

10. Imprint

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