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FMC SFP Adapter

DS#T0012 REV 2026/11/27
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SFP Adapter Board for Low-Pin Count FMC Connectors

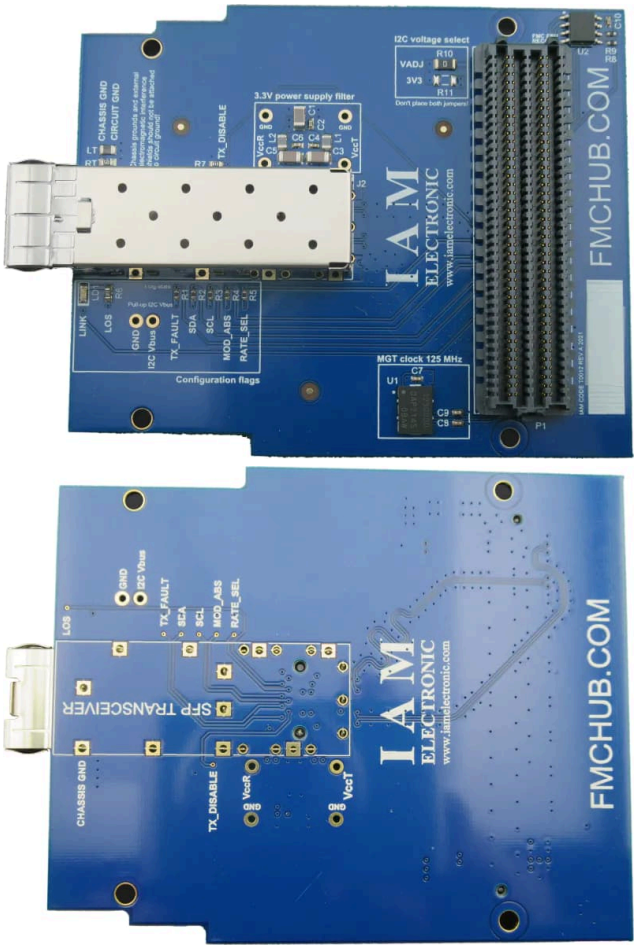
Features

- SFP+ connector and cage
- Tested up to 12.5 Gb/s without bit errors
- ANSI/VITA 57.1 compliant
- Commercial grade form factor
- Low-pin count (LPC) connector
- Fits any LPC or HPC carrier (LPC subset on HPC)
- 125 MHz reference clock on board
- LED for link status
- EEPROM for FRU information storage
- Selectable pull-up voltage for I2C and control signals (VADJ or 3P3V)
- Open-source hardware

Applications

- 1000BASE-X data links
- Board-to-board connections
- Testing and debugging of SFP transceivers
- Easy prototyping
- Loopback testing
- Research and education with FPGAs

FMC SFP Adapter Board



1. Description

The **FMC SFP Adapter Board** is an adapter for accessing the multi-gigabit transceiver data pair of the FMC low-pin count (LPC) connector. The DP0_C2M and DP0_M2C data pairs are connected to the 20-pin SFP board connector inside the single-port SFP+ cage. The board has been tested without bit errors up to 12.5 Gb/s and suits SFP+ (10GBASE-R) and 1000BASE-X applications (Ethernet transmission over fibre). An on-board oscillator provides a reference clock of 125.000 MHz to the GBTCLK signal pair (clock signal for multi-gigabit transceiver data pair). All electrical signals of the SFP transceiver are accessible via the FMC-LPC connector or test points on

the PCB. No configuration of the card is necessary for easy startup. The board fits any LPC or HPC carrier: on an HPC carrier it uses the LPC subset of the pins.

2. Application information

2.1 Fibre link between two carriers

The boards can be used in a loopback test to check the components of a board-to-board connection. These tests are useful for evaluating an FPGA test design on a carrier board, or for transceiver tests. We have tested the FMC SFP adapter with various SFP optical transceivers.

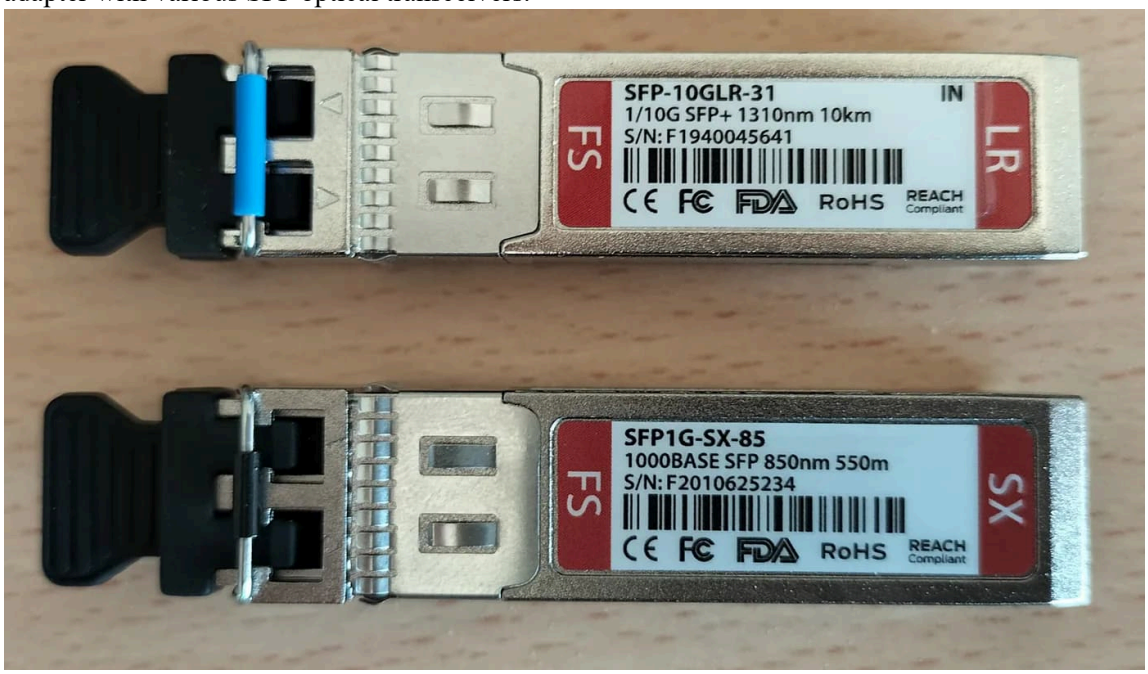


Fig. 1: SFP transceivers used for testing the FMC SFP adapter.

Our tests have been carried out with two FMC carrier boards with Xilinx FPGAs (fig. 2). We use the Xilinx IBERT core for loopback testing. The "far end PMA" loopback mode must be enabled on one of the boards.

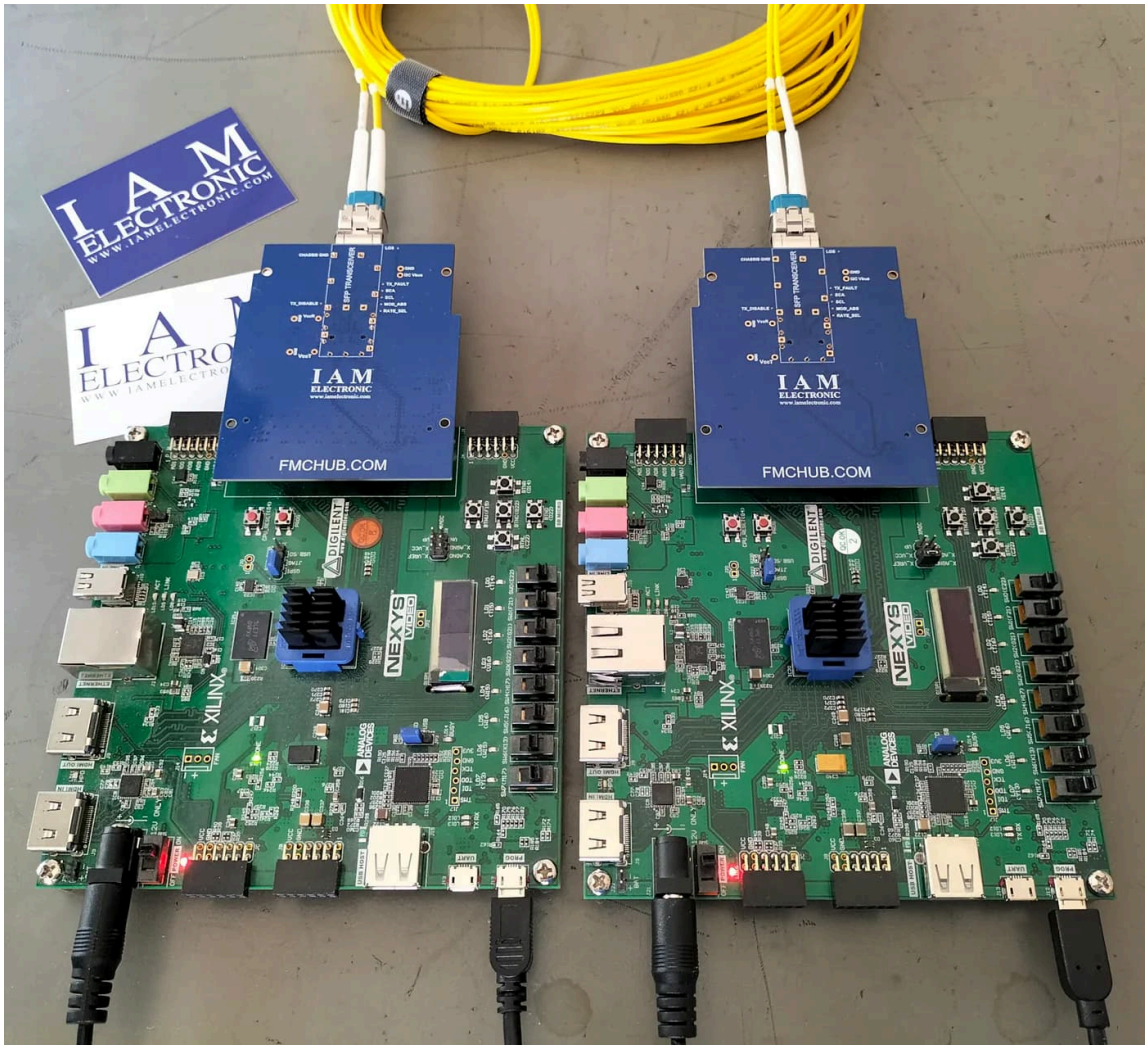


Fig. 2: FMC loopback configuration with two carrier boards and two FMC SFP adapter modules.

The eye diagrams for different transceivers and data rates are shown in fig. 3 to fig. 5.

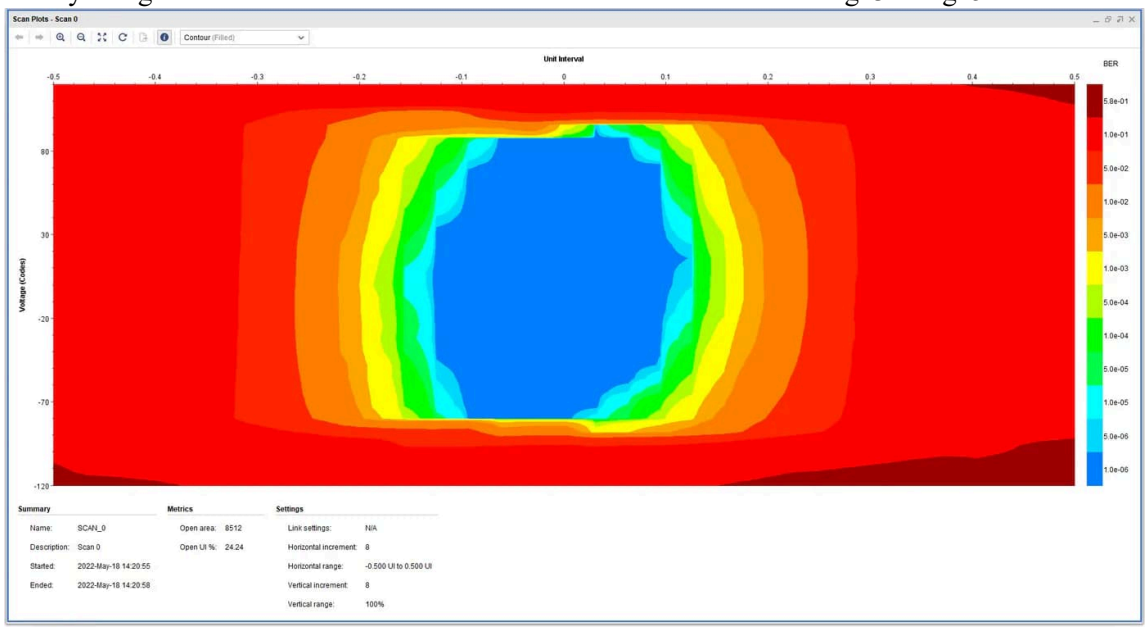


Fig. 3: Eye diagram from Xilinx IBERT with 1000BASE SFP Transceivers in loopback configuration with 1.25 Gb/s.

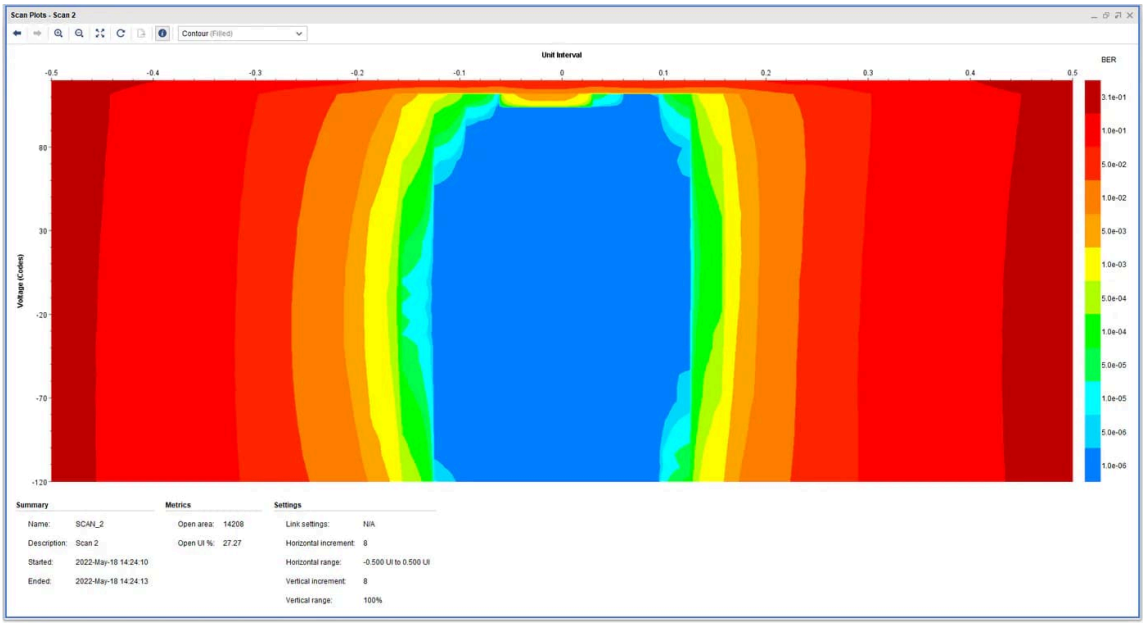


Fig. 4: Eye diagram from Xilinx IBERT with 10G SFP+ Transceivers in loopback configuration with 1.25 Gb/s.

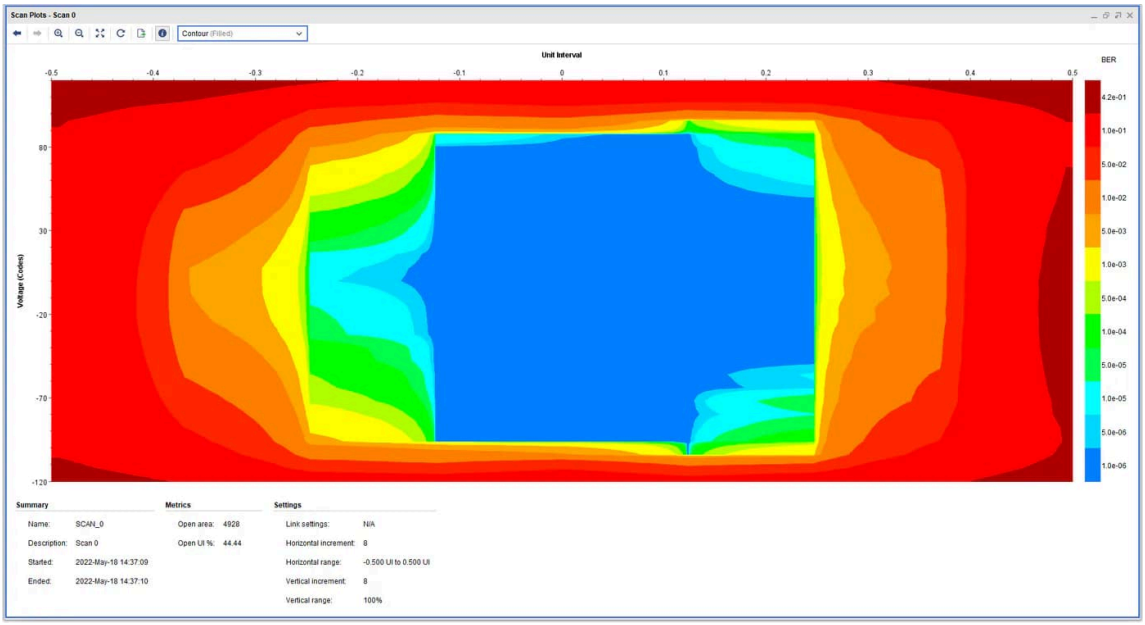


Fig. 5: Eye diagram from Xilinx IBERT with 10G SFP+ Transceivers in loopback configuration with 3.75 Gb/s.

During all tests, we did not receive a single bit error. The bit error rate (BER) was also checked with the Xilinx IBERT core (fig. 6).

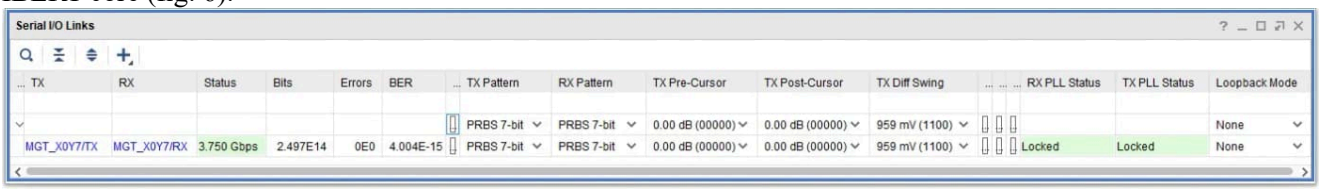


Fig. 6: The bit error rate of the FMC SFP adapter with a 10G SFP+ transceiver in loopback mode at 3.75 Gb/s.

2.2 SFP loopback test up to 12.5 Gb/s

The adapter was tested on a prototype of the MANZA DUO carrier with a Kintex UltraScale+ XCKU3P FPGA (GTY transceivers) in FMC port J1. A passive SFP28 loopback module (FS SFPLOOP-25G) in the cage connects TD to RD, so the transmitter of the FPGA lane feeds its own receiver. The test used the AMD IBERT core, default transceiver settings without tuning and a PRBS checker (tab. 1). A bit count N without errors bounds the bit error rate below 3/N with 95 % confidence. 12.5 Gb/s is the highest line rate of the GTY transceivers in the package of this FPGA, so the limit of the adapter was not reached.

Tab. 1: SFP loopback results.

Line rate	Pattern	Reference clock	Bits	Errors	BER (95 %)
12.5 Gb/s	PRBS-31	125 MHz, adapter	3.0E13	0	< 1E-13
12.5 Gb/s	PRBS-7	125 MHz, adapter	3.0E12	0	< 1E-12
12.5 Gb/s	PRBS-31	125 MHz, carrier	3.0E12	0	< 1E-12
10.3125 Gb/s	PRBS-31	156.25 MHz, carrier	3.1E12	0	< 1E-12
10.3125 Gb/s	PRBS-7	156.25 MHz, carrier	3.1E12	0	< 1E-12
8.5 Gb/s	PRBS-31	125 MHz, adapter	3.1E12	0	< 1E-12
8.5 Gb/s	PRBS-7	125 MHz, adapter	3.1E12	0	< 1E-12
8.5 Gb/s	PRBS-31	125 MHz, carrier	3.1E12	0	< 1E-12
6.25 Gb/s	PRBS-31 / PRBS-7	125 MHz, adapter	3.0E12 each	0	< 1E-12
6.25 Gb/s	PRBS-31	125 MHz, carrier	3.0E12	0	< 1E-12
5.0 Gb/s	PRBS-31 / PRBS-7	125 MHz, adapter	3.0E12 each	0	< 1E-12
5.0 Gb/s	PRBS-31	125 MHz, carrier	3.0E12	0	< 1E-12
3.75 Gb/s	PRBS-31 / PRBS-7	125 MHz, adapter	3.0E12 each	0	< 1E-12
3.75 Gb/s	PRBS-31	125 MHz, carrier	3.0E12	0	< 1E-12

The on-board 125 MHz oscillator serves as the transceiver reference clock for 1.25, 2.5, 3.125, 3.75, 5.0, 6.25, 8.5 and 12.5 Gb/s (tested from 3.75 to 12.5 Gb/s). 10.3125 Gb/s (10GBASE-R) cannot be derived from 125 MHz with an integer PLL setting; use a 156.25 MHz clock from the carrier.

Tab. 2 lists the horizontal eye opening at the FPGA receiver after the complete loop (carrier, adapter and loopback module), PRBS-31, default settings, measured on one unit. Fig. 7 shows the eye scan at 12.5 Gb/s with the reference clock of the adapter.

Tab. 2: Horizontal eye opening at a BER of 1E-6.

Line rate	Eye opening
12.5 Gb/s	0.45 to 0.49 UI
10.3125 Gb/s	0.62 UI
8.5 Gb/s	0.63 UI
6.25 Gb/s	0.57 UI
5.0 Gb/s	0.68 to 0.70 UI
3.75 Gb/s	0.77 UI

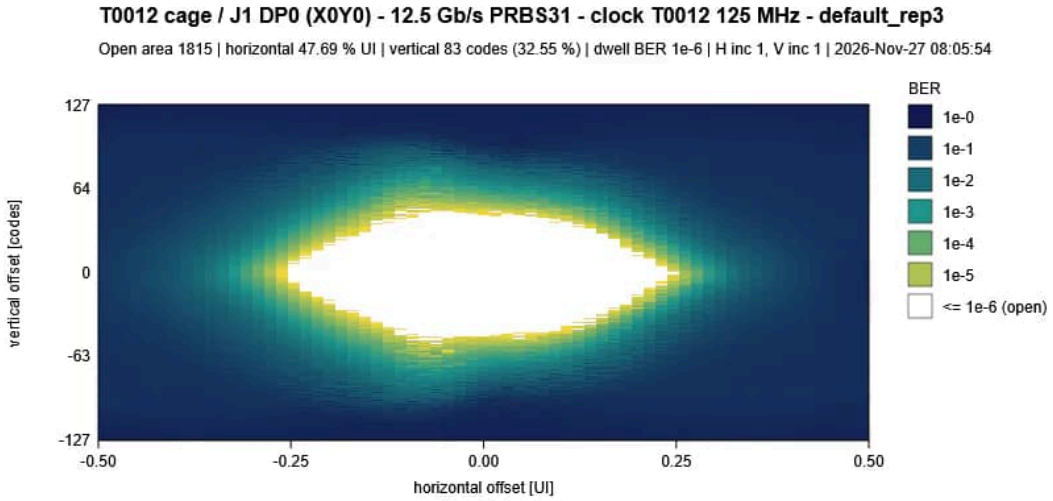


Fig. 7: Eye scan of the SFP loopback at 12.5 Gb/s, PRBS-31, reference clock from the 125 MHz oscillator of the adapter.

Fig. 8 to fig. 12 show lane DP0 at the other rates.

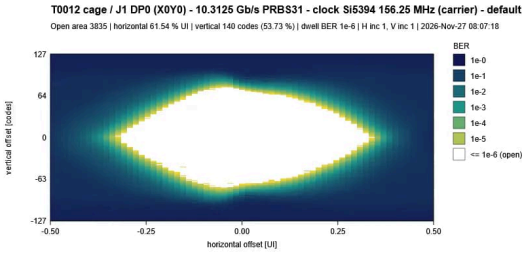


Fig. 8: SFP loopback at 10.3125 Gb/s, PRBS-31, carrier clock 156.25 MHz.

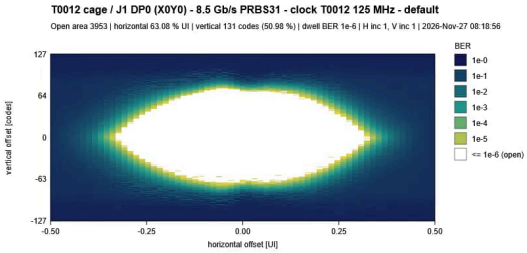


Fig. 9: SFP loopback at 8.5 Gb/s, PRBS-31, adapter clock 125 MHz.

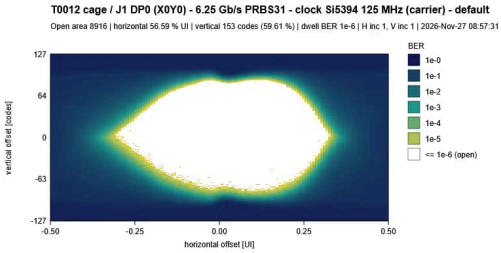


Fig. 10: SFP loopback at 6.25 Gb/s, PRBS-31, carrier clock 125 MHz.

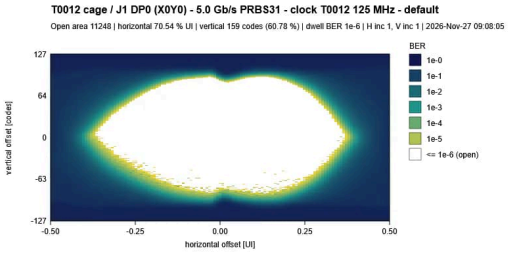


Fig. 11: SFP loopback at 5.0 Gb/s, PRBS-31, adapter clock 125 MHz.

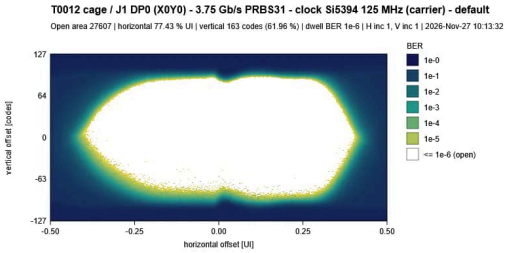


Fig. 12: SFP loopback at 3.75 Gb/s, PRBS-31, carrier clock 125 MHz.

3. Electrical data (pin description)

The printed circuit board is open-source hardware! You can download the FMC SFP Adapter board schematics and PCB layout files in their latest revision from the GitHub repository.

3.1 Pinout of the FMC LPC Connector

Fig. 13 and tab. 3 show the connections of the signals on the FMC connector P1.

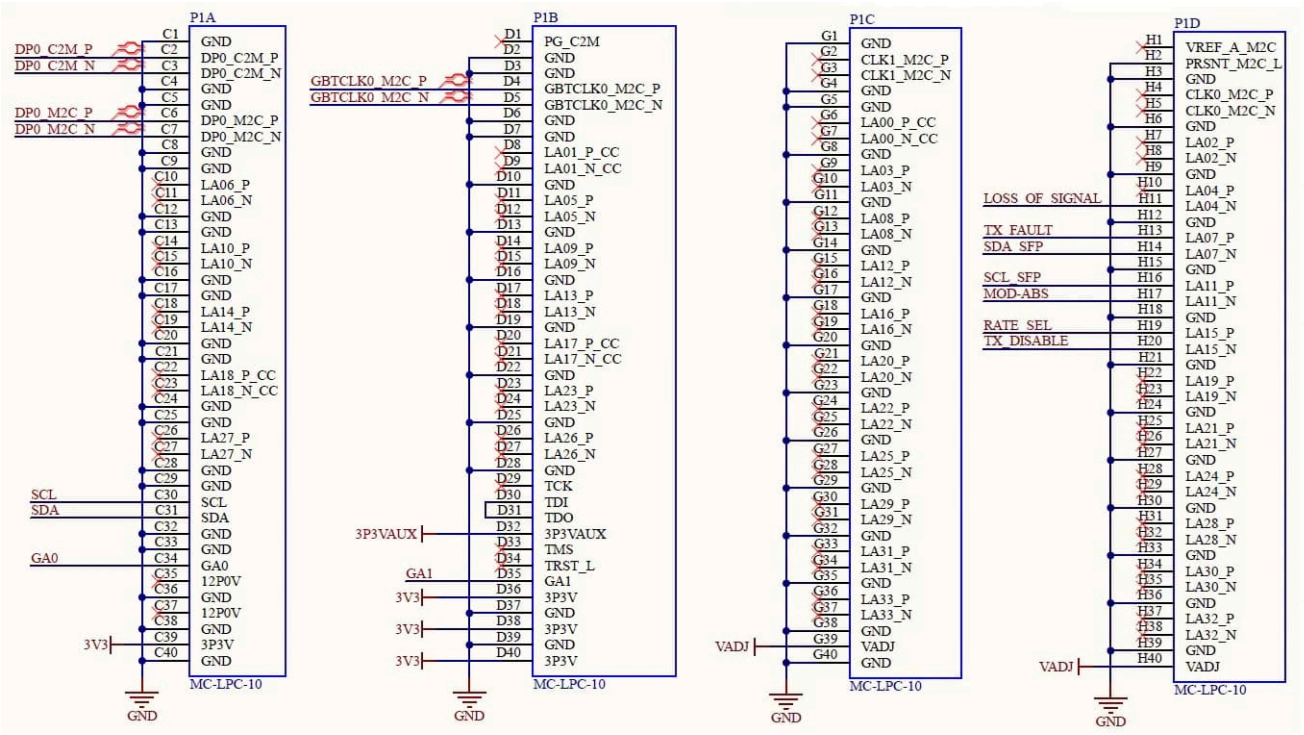


Fig. 13: Pin assignments of the FMC LPC connector P1.

Tab. 3: Pin assignments of the FMC SFP Adapter Board.

FMC pin name	FMC pin designator	SFP pin name
LA04_N	H11	LOS (LOSS OF SIGNAL)
LA07_P	H13	TX_FAULT
LA07_N	H14	SDA
LA11_P	H16	SCL
LA11_N	H17	MOD-ABS
LA15_P	H19	RS0 (RATE SELECT)
LA15_N	H20	TX_DISABLE
DP0_C2M_P	C2	TD+
DP0_C2M_N	C3	TD-
DP0_M2C_P	C6	RD+
DP0_M2C_N	C7	RD-
GBTCLK0_M2C_P	D4	125 MHz clock + (to FPGA)
GBTCLK0_M2C_N	D5	125 MHz clock − (to FPGA)

3.2 SFP control signals and LED

The control signals TX_FAULT, SDA, SCL, MOD-ABS and RATE_SEL (RS0) have 4K7 pull-up resistors (R1 to R5) on the board. Their voltage is selected with a zero-ohm resistor: R10 connects the pull-ups to VADJ (fitted by default), R11 to 3P3V. Do not place both resistors. TX_DISABLE is pulled low with 1 kΩ (R7), so the transmitter is on by default; RATE_SEL is pulled high, which selects full bandwidth. The blue LED LD1 (LINK) is connected to LOS through 100 Ω (R6) and lights while LOS is low, that is while the transceiver receives a signal.

3.3 Clock, data lanes, supply and fixed connections

The 125.000 MHz reference clock comes from the oscillator U1 (DSC1103AI5-125.0000). It is AC-coupled on the board with 100 nF capacitors (C8, C9); the termination is on the FPGA carrier. The data lanes DP0_C2M and DP0_M2C are routed to the SFP board connector without coupling capacitors, as the SFP transceiver is AC-coupled inside. The transceiver supplies VccT and VccR are taken from 3P3V, each through a filter of 1 µH (Murata LQM21PN1R0MC0D, rated 0.8 A at 85 °C, max. 0.238 Ω), 22 µF and 100 nF. The JTAG chain is closed on the board (TDI connected to TDO), and PRSNT_M2C_L is connected to GND.

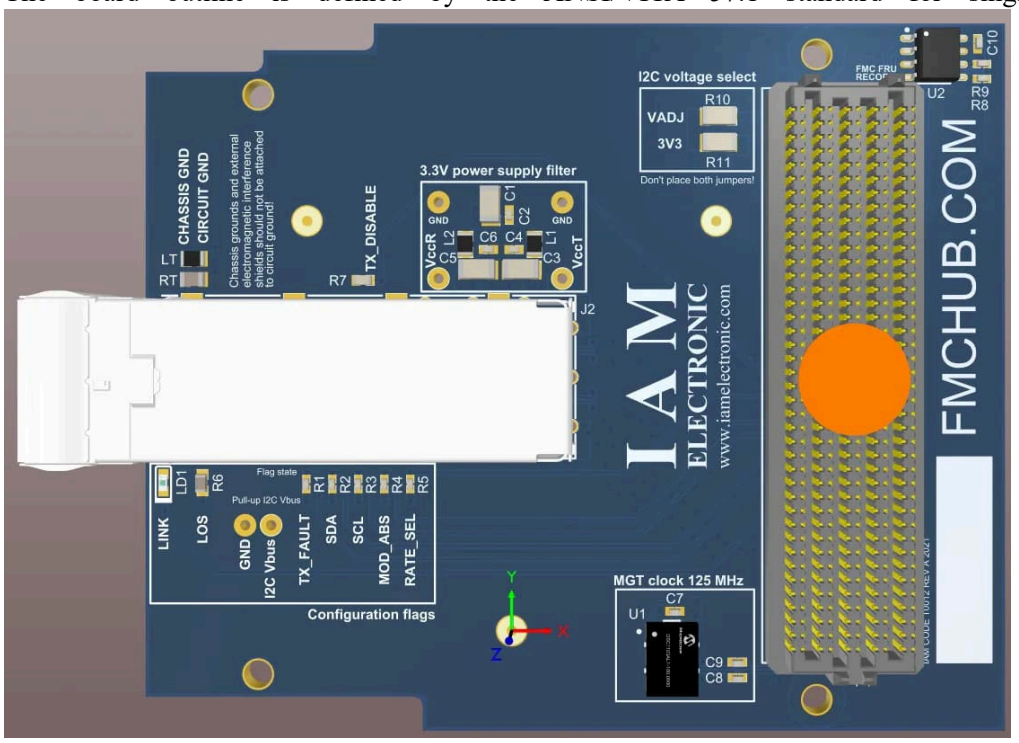
SFP+ board connector: TE 1888247-2. SFP+ cage: Molex 74754-8101. Boards of earlier production runs carry the SFP board connector TE 1367073-1 and the SFP cage Molex 74754-0101.

3.4 FMC FRU EEPROM

The EEPROM for storing FMC FRU (field replaceable unit) information is an M24C02 with 2 Kbit (256 Byte). The FRU record determines the voltage on the VADJ rail of the FMC connector. By default, the FRU EEPROM is programmed to request 3.3 V from the carrier board. Further, the memory stores the board information such as manufacturer name and product number. The device can be read and written by the I2C interface of the FMC connector (pins C30 and C31). The EEPROM is supplied from 3P3VAUX, and the FMC SFP Adapter Board includes 4K7 pull-up resistors to 3P3VAUX on the SCL and SDA signal lines. The write control input WC is tied to GND, so the EEPROM can be written. The I2C address of the M24C02 is defined by the GA0 and GA1 pins of the FMC connector in accordance with the ANSI/VITA 57.1 standard.

4. Mechanical data

The board outline is defined by the ANSI/VITA 57.1 standard for single width FMC modules.



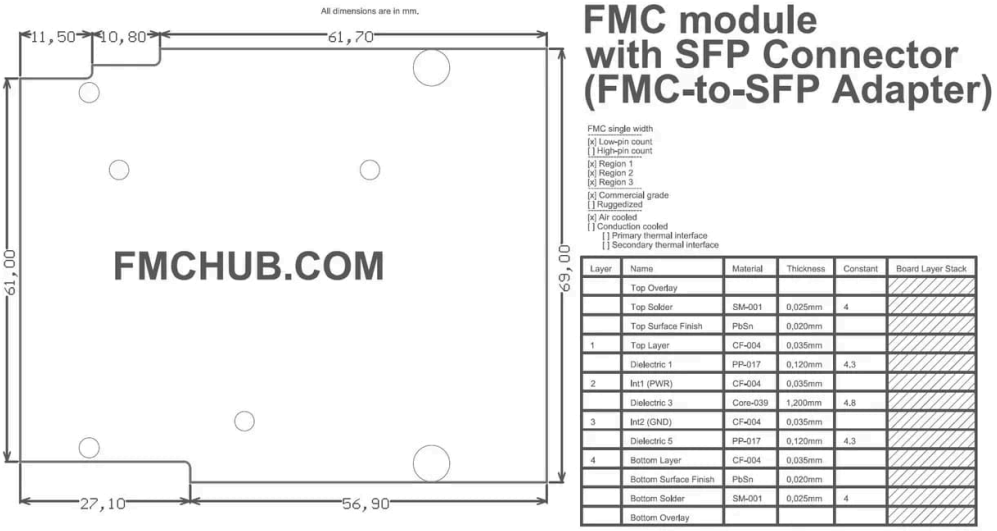


Fig. 14: Mechanical drawing of the FMC SFP Adapter board.

The mounting holes are plated but have no electrical connection. Their sizes and positions are in accordance with ANSI/VITA 57.1 single width FMC modules.

5. Ordering information

The FMC SFP Adapter Board can be ordered at various online market places, or you can request a quotation by sending an e-mail to info@iamelectronic.com.

Tab. 4: Assembly variants of FMC SFP Adapter board with product numbers and market places.

Product no.	Description	Market place	Request quote	Standard lead time
T0012	FMC LPC SFP Adapter Board with MC-LPC-10 connector, SFP+ connector with cage and clock generator on bottom side.	IAM Electronic Shop Ebay #185439240058 Tindie #26891 DigiKey 6068-T0012-ND	info@iamelectronic.com	Normally in stock, otherwise 3 weeks

6. Resources

[1] Schematics: FMC_SFP_ADAPTER.pdf
[2] Github repository: https://github.com/FMCHUB/FMC_SFP_ADAPTER

7. Document history

Document number:
DS#T0012

Version history:
2026/11/27: SFP+ connector and cage. Added: SFP loopback test from 3.75 to 12.5 Gb/s with eye scans, control signals and LED, clock, supply, LPC/HPC compatibility. Corrections in tab. 1, numbering, dates of the version history, links
2022/05/24: Update links for schematics and Github repository, Ebay and Tindie article listings
2022/05/19: New content in section mechanical data
2022/05/19: New content in section application information (1. loopback test)
2022/05/18: Initial release