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FMC Loopback Module

DS#T0007 REV 2026/11/23
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FPGA Mezzanine Card (FMC) Loopback Module

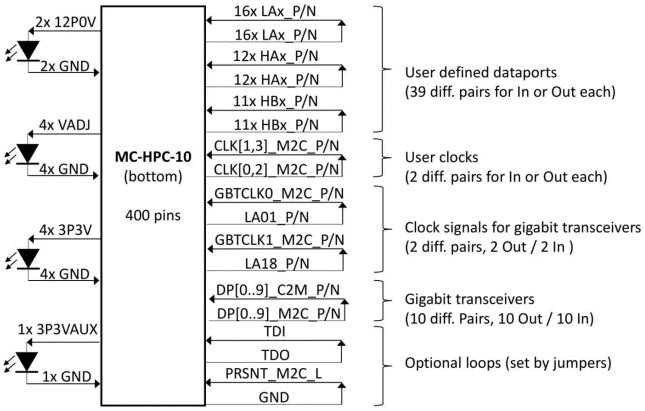
Features

- Passive plug-in module, no configuration required
- Transceiver loops operated error-free at up to 12.5 Gbit/s (DC-coupled loops, see section 2.3)
- 11x LEDs for visual feedback of the applied supply voltages
- High-Pin Count (HPC) connector according to ANSI/VITA 57.1 FMC
- Mates with HPC or LPC carrier boards
- All FMC data and clock pins are completely controlled by the FPGA
- Optional pin header (2.54 mm pitch) for voltage monitoring
- Practical design for the best price-performance ratio
- 2-layer printed circuit board (PCB)
- Reference designs are available
- Open source hardware

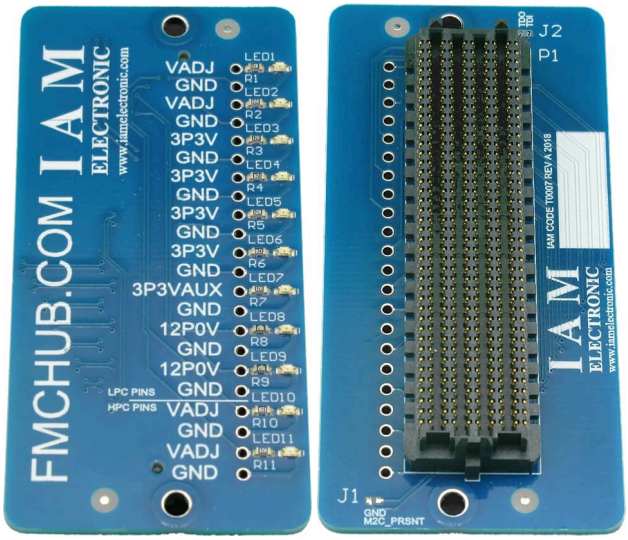
Applications

- Easy prototyping and analysis of high-speed data links
- Testing and debugging FMC carrier boards
- Fast verification of signal integrity on FMC carrier boards
- Research and education with FPGAs

Block diagram



The photos below show the top side with LEDs to indicate applied voltages and bottom side with HPC mezzanine card connector (MC-HPC-10).



Top side Bottom side

1. Description

The **FMC Loopback Module** is a passive plug-in adapter for ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) connectors. The loopback board is designed to mate a High-Pin Count (HPC) connector, but also fits without restrictions to Low-Pin Count (LPC) connectors. According to the FMC standard, all signals of an FPGA are connected by the mezzanine board as loopback. This means that each pin of an IO bank has a fixed endpoint through the FMC loopback card. These signal pairs must be defined as In/Out pairs in the FPGA on the carrier side. Apart from that necessary IO constraints, the FMC Loopback Board does not require any further configuration for its full functionality.
An FMC loopback test of an FMC carrier board is essential to identify production faults (e.g. defective solder joints of the FPGA package or FMC connector). In addition to production tests, a loopback test reveals information about the signal integrity on the carrier board (e.g. by eye scans). Finally, the FMC loopback module can be used to implement high-speed data links at an early prototyping stage, where the transmitter and receiver logic is controlled by a single FPGA. Such a performance test can be used to determine latency, throughput or data loss of high-speed serial data links (e.g. JESD204B).

Update 2026/11: The transceiver loops of the module are direct TX-to-RX connections without coupling capacitors (DC-coupled). In this mode the module has been operated error-free at up to 12.5 Gbit/s (PRBS-31) on an AMD Kintex UltraScale+ GTY carrier. The FMC Loopback Module is a functional loopback and stress test for the transceiver lanes. It is not a signal-integrity reference. Details are given in section 2.3.

2. Application information

The FMC loopback module is suitable for checking the user-defined data signals (LA, HA or HB bank signals), the user clock signals (CLKx_M2C_P/N, CLKx_C2M_P/N) or the multi-gigabit transceiver signals (DPx_C2M_P/N, DPx_M2C_P/N) with the corresponding clock signals (GBTCLKx_M2C_P/N). Depending on which FMC connector is used on the carrier, the pins available for a loopback test must be selected accordingly. In almost all cases the carrier has a fully occupied connector according to ANSI/VITA 57.1 LPC definition.

2.1 Low-Pin count (LPC) connector loopback

The pins used by the LPC connector are a subset of the High-Pin count (HPC) connector's pins. There are in total 34 differential pairs for user data (LAx_P/N pins), 2 diff. pairs dedicated to user clock signals, 1 multi-gigabit transceiver consisting of 1 diff. TX pair (DP0_M2C_P/N) and 1 diff. RX pair (DP0_C2M_P/N) with corresponding reference clock (GBTCLK0_M2C_P/N). All these signals can be used in a loopback test. Optionally, the JTAG pins TDI and TDO can be short-circuited on the PCB and the PRSNT_M2C_L signal can be connected to GND. A typical application with an LPC carrier board is shown below.

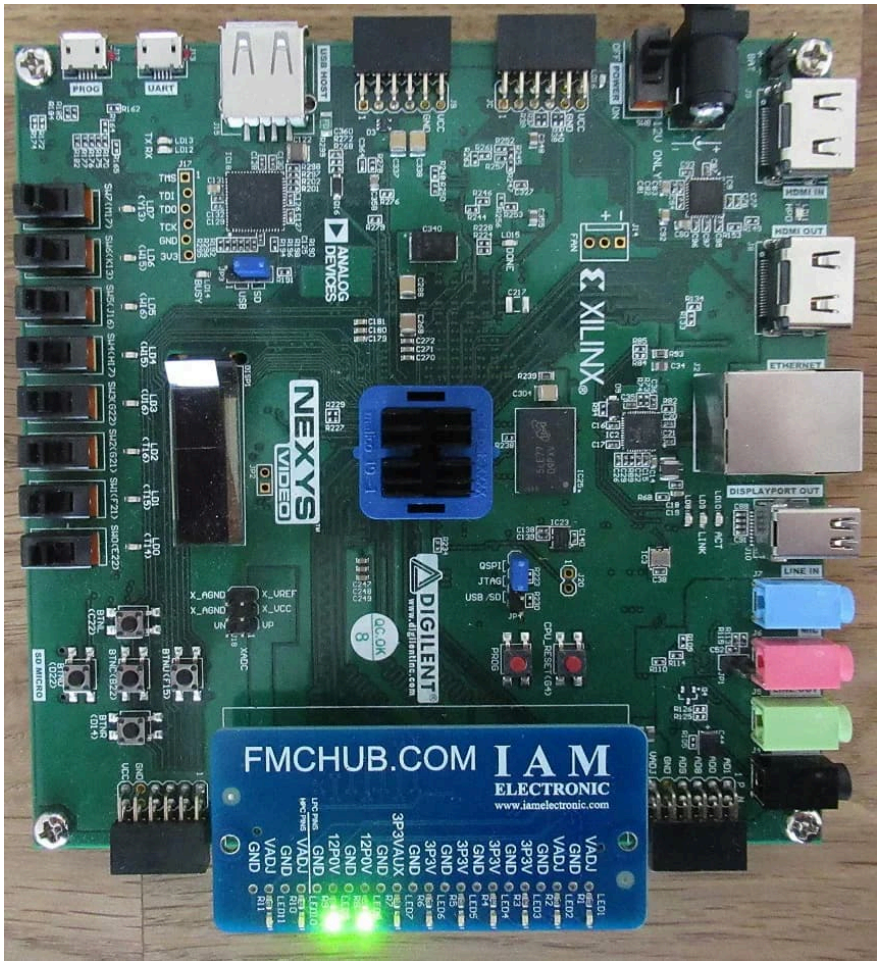


Fig. 1: FMC Loopback Module plugged on LPC carrier board (Digilent Nexys Video™ Board, 410-316).

Some carrier boards require the PRSNT_M2C_L pin to be pulled down, indicating that a mezzanine module is present and therefore supply voltages may be activated or adjusted. In case that all supply voltages are switched on by the carrier, the FMC loopback card's LEDs will light up. Fig. 1 shows the case where the carrier board is switched off, but the 12 V supply rail still supplies the LEDs, because the DC power supply is plugged into the board. After the carrier is switched on, the following situation occurs.



Fig. 2: FMC Loopback Module plugged on switched on LPC carrier board.

Please note that the voltage pins VADJ (2x on the LPC connector, 4x in total on a HPC carrier) are an adjustable voltage level from the carrier to the mezzanine card in the range of 0 .. 3.3 V. Typical values are 1.2 V, 1.8 V, 2.5 V or 3.3 V. In case the voltage VADJ is set below the LEDs forward voltage of 2.1V the LEDs associated to these pins (LED1, LED2, LED10, LED11) will not light up. To check the correct voltage level, you must measure directly at the test points next to the LEDs with a voltmeter.

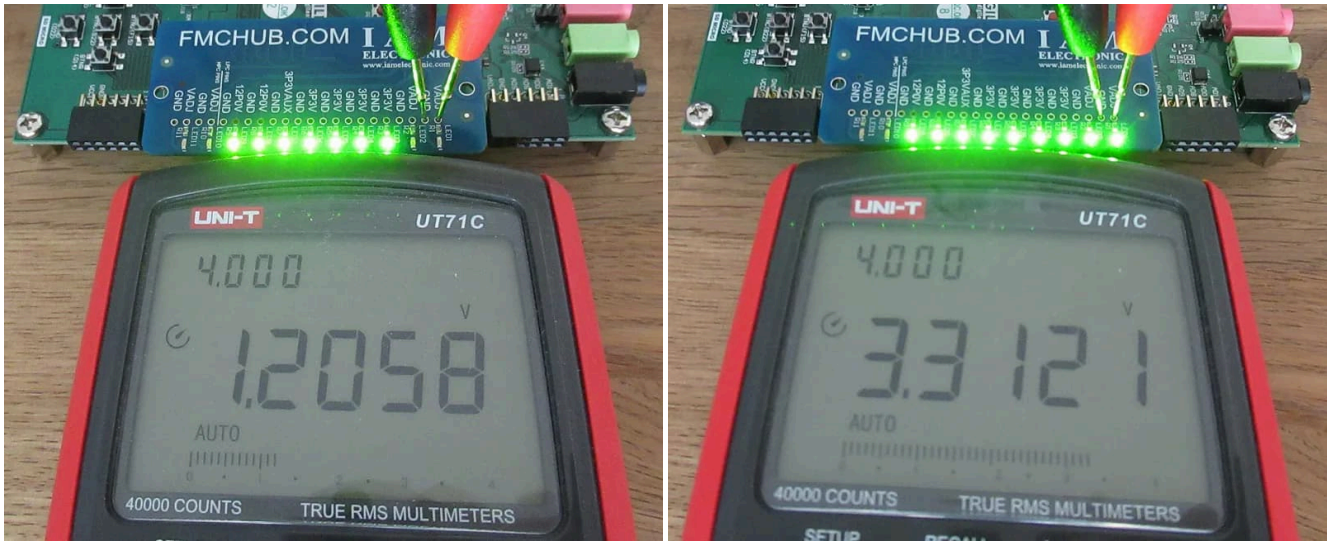


Fig. 3: FMC Loopback Module plugged on LPC carrier board with too low voltage level on VADJ pins (left) and sufficient voltage level (right).

An important detail is that **the GND pins on the loopback bard are not tied together**! In case an LED does not light up, the reason is either a low voltage, a defective voltage pin or a defective GND pin on the carrier (device under test)!
The test of the supply voltages with the LEDs gives a first quick impression about possible errors of the DUT. A test of the data lines gives of course a much more detailed insight into the correct function, and should be always carried out. Fig.4 shows an overview of the available data lines of an LPC carrier with attached FMC loopback board.

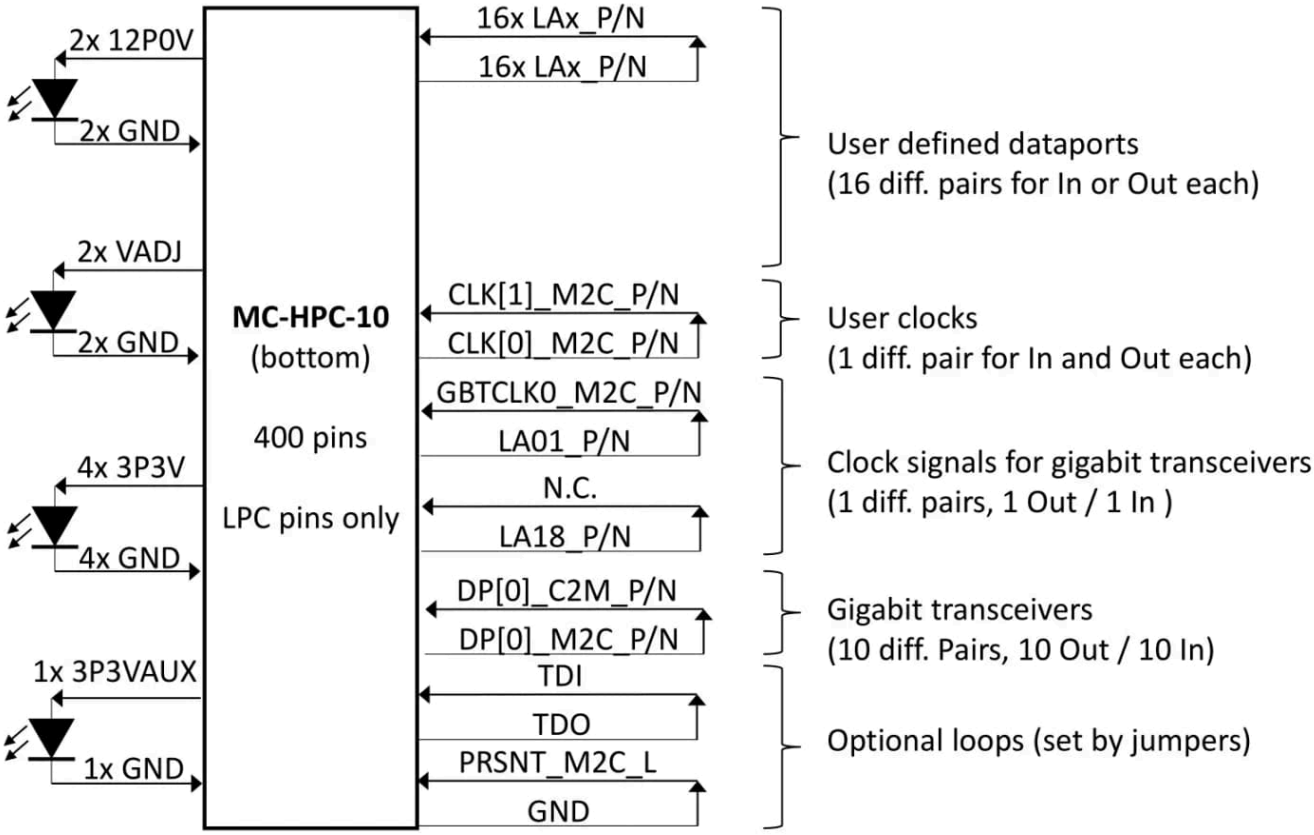


Fig. 4: Blockdiagram of the FMC Loopback Module's Low-Pin-Count (LPC) pins. This is only a subset of all available pins on the board.

Please note that in an LPC only configuration, the user data pair LA18_P/N has no endpoint, because the target pins GBTCLK1_M2C_P/N are located in the HPC rows of the connector.
Furthermore it has to be mentioned that a clocking of the Gigabit-transceiver by FPGA output pins does not achieve best performance. But in order to keep the operation of the board as simple as possible, we have chosen to provide an internal clock generation by the FPGA over a programmable external clock source. So the user don't have to deal with other devices and can stick to the same FPGA device. This approach provides maximum flexibility in clock

generation and also allows data rates up to 10 Gbit/s (see section 2.2 HPC loopback).

2.1.A Eye-scan reference design with clock from silicon MEMS oscillator

Board:	Digilent Nexys Video Artix-7 FPGA
FPGA:	Xilinx XC7A200T-1SBG484C
Repository / Download:	https://www.github.com/fmchub
Notes:	Reference clock is 135 MHz generated by external oscillator on carrier board

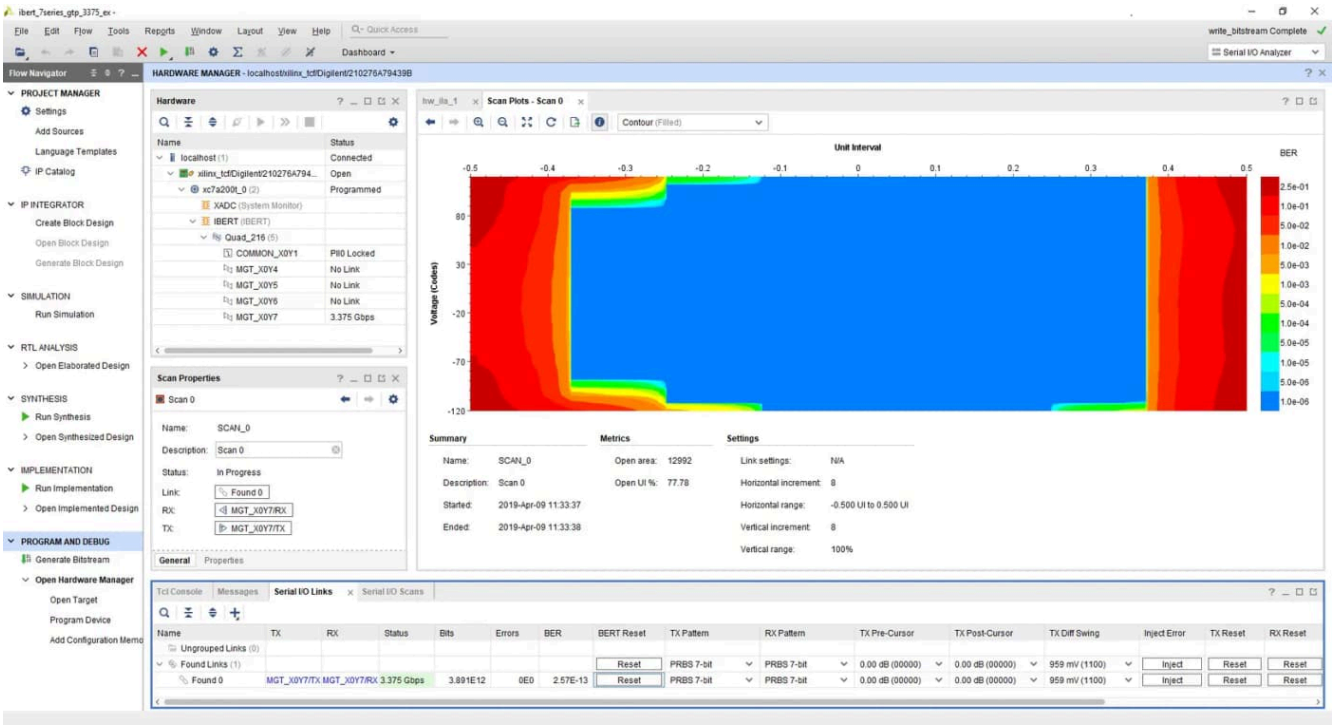


Fig. 5: Eye scan with Xilinx IBERT core at 3.375 Gbit/s and reference clock from silicon MEMS oscillator (135 MHz)

2.1.B Eye-scan reference design with clock from built-in Xilinx PLL

Board:	Digilent Nexys Video Artix-7 FPGA
FPGA:	Xilinx XC7A200T-1SBG484C
Repository / Download:	https://www.github.com/fmchub
Notes:	Reference clock is 125 MHz generated by built-in Xilinx PLL out of 100 MHz clock. The generated clock is output by the FPGA via pins LA01_P/N and routed to pins GBTCLK0_M2C_P/N through the loopback adapter.

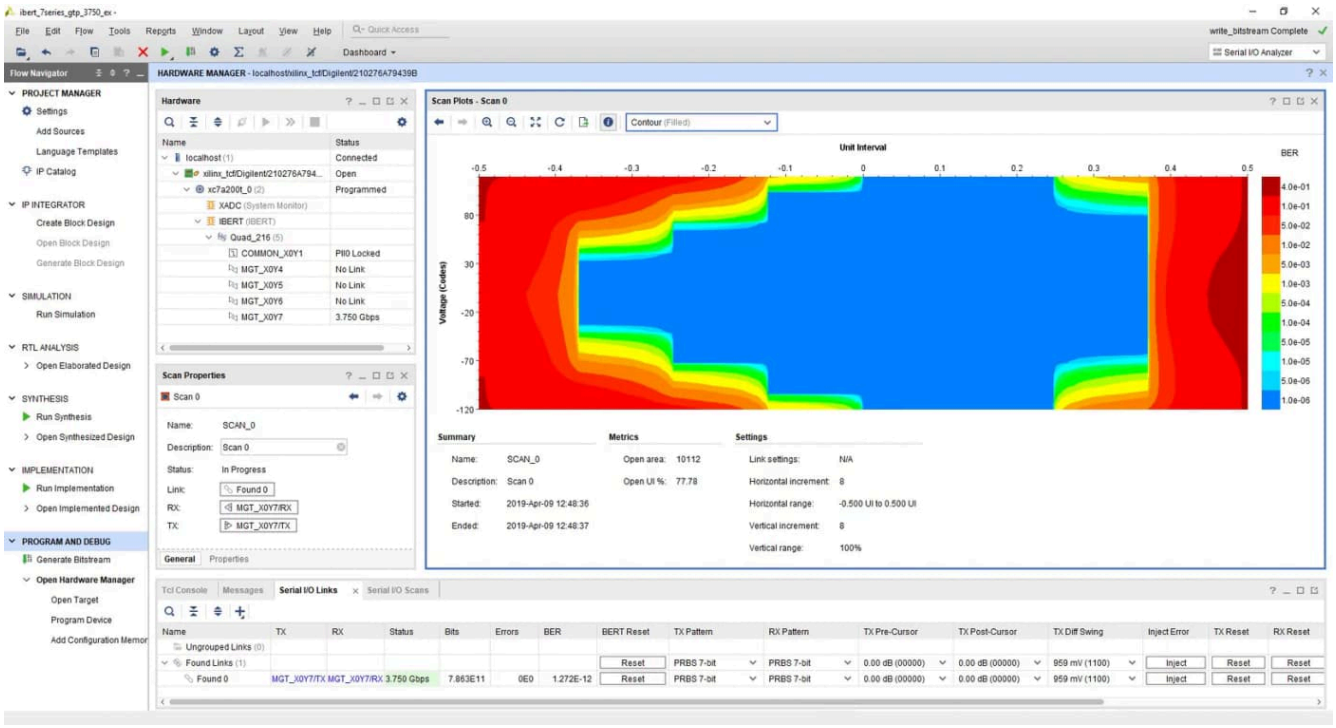


Fig. 6: Eye scan with Xilinx IBERT core at 3.750 Gbit/s and reference clock from built-in Xilinx PLL (125 MHz).

2.1.B Loopback pattern reference design

Board:	Digilent Nexys Video Artix-7 FPGA
FPGA:	Xilinx XC7A200T-1SBG484C
Repository / Download:	https://www.github.com/fmchub
Notes:	Use SW0 and BTNC of the board to control pattern generator: SW0='1': All Ones Pattern, all LEDs must light up SW0='0': Press and hold BTNC, running LEDs light up when all patterns are successful

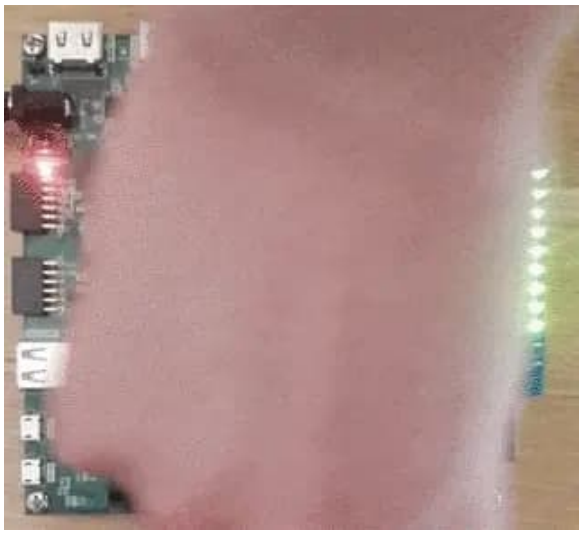


Fig. 7: Loopback demo with pattern generator. The LEDs of the carrier board show the correct function.

2.2 HPC loopback

Since the LPC connector is a subset of the HPC connector, all previous instructions also apply to the HPC connector. Looking at the power test with the LEDs, this time of course all LEDs must light up if the VADJ voltage reaches a valid voltage level. Below is an example application where the FMC loopback board is attached to an FMC HPC carrier board (Avnet UltraZed-EV with Carrier Card).

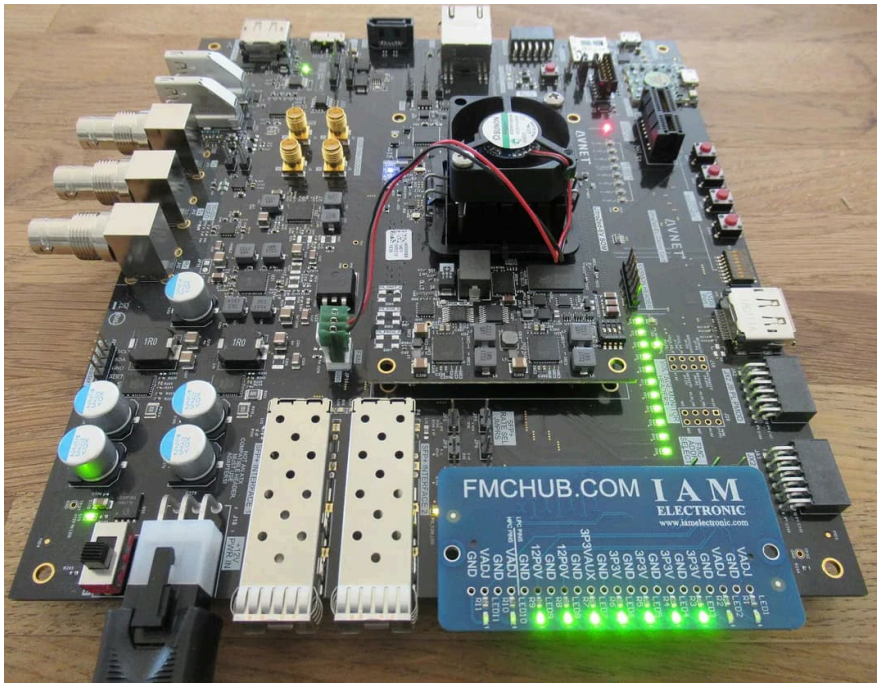


Fig. 8: FMC Loopback Module plugged on HPC carrier board (Avnet UltraZed-EV with Carrier Card).

Even if the adjustable voltage is for that example below the forward voltage of the LEDs (2.1 V), you can still see a dimmed light.

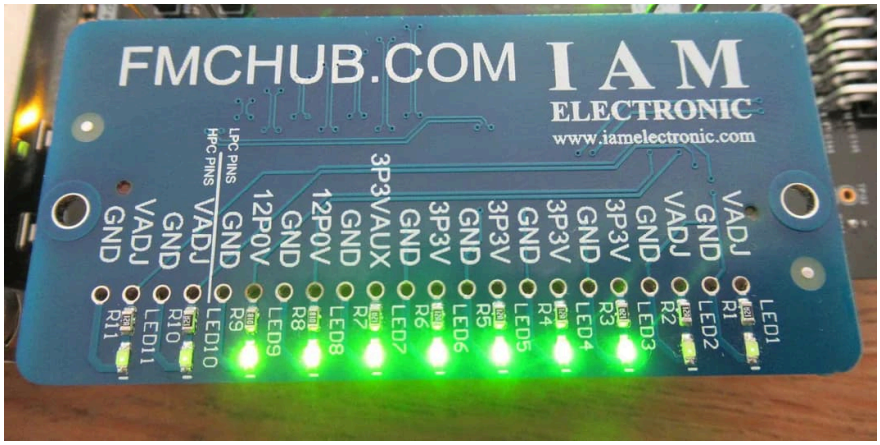


Fig. 9: FMC Loopback Module plugged on HPC carrier board with VADJ of 1.8 V. A dimmed light of the LEDS (LED1, LED2, LED10, LED11) is visible.

The HPC connector has in total 160 user data lines, that is 80 differential pairs. Two of them, LA01_P/N and LA18_P/N, are routed to the reference clock inputs of the transceivers, GBTCLK0_M2C_P/N and GBTCLK1_M2C_P/N: a carrier can drive them, but it has no general-purpose input there. The remaining 78 pairs form 39 loops from pair to pair (16 in the LA group, 12 in HA and 11 in HB), so a loopback application has 39 differential pairs for transmitting data and 39 for receiving data. Additionally there are 10 multi-gigabit transceivers (10 transmitter and 10 receiver pairs). The user clocks are looped as well: CLK0_M2C with CLK1_M2C and CLK2_BIDIR with CLK3_BIDIR. The block diagram in fig. 9 gives a schematic overview of all signals.

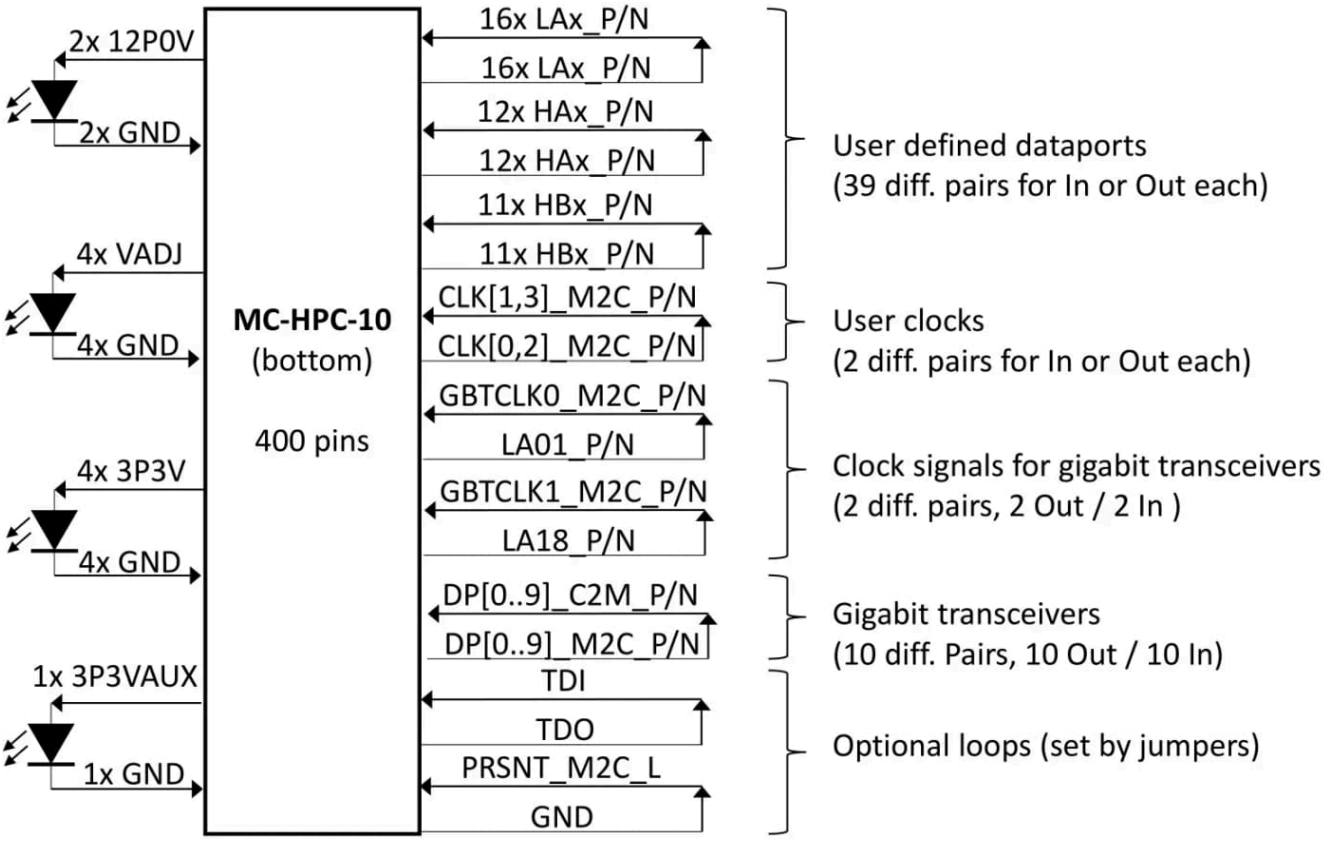


Fig. 10: Blockdiagram of the FMC Loopback Module's High-Pin-Count (HPC) pins.

With Xilinx IBERT core, the FMC loopback module achieves a throughput of 10 Gbit/s per MGT lane, which is in total 8x 10 Gbit/s. The HPC carrier does only provide 8 out of 10 MGT lanes.

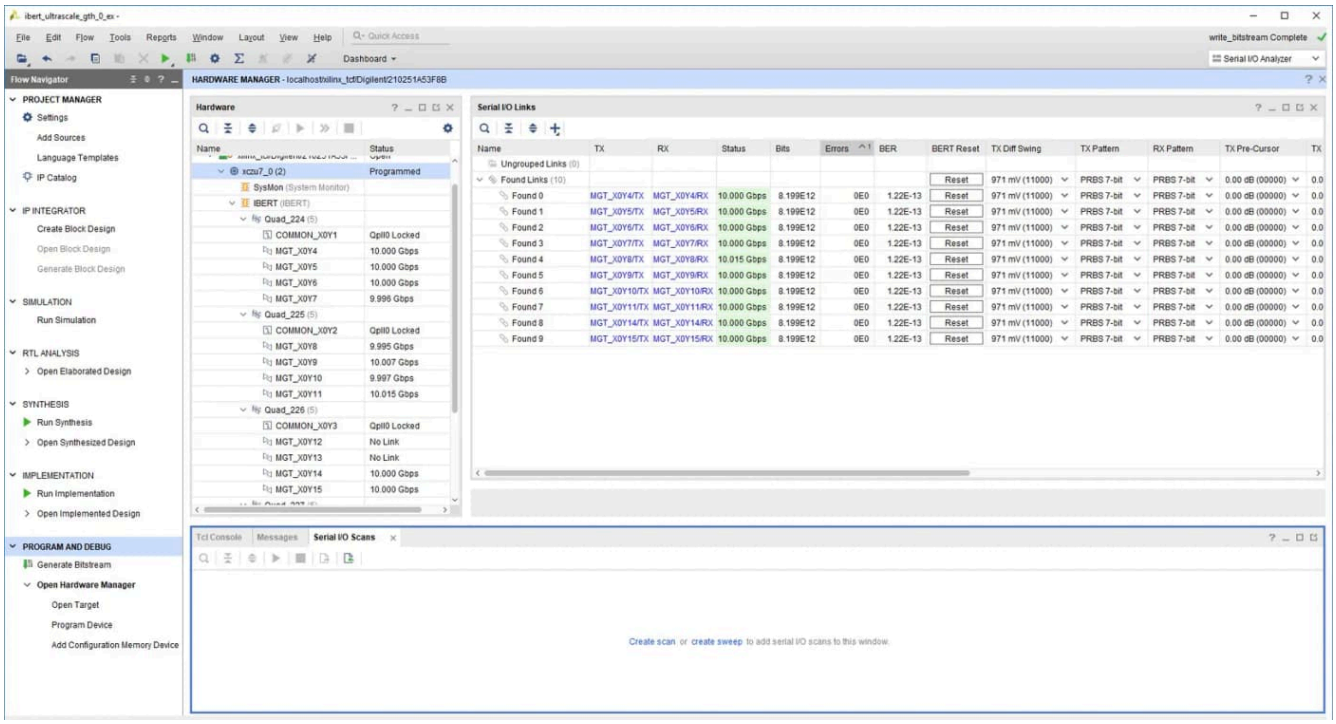


Fig. 11: The FMC Loopback Module is capable of a maximum throuput of 8x 10 Gbit/s over multi-gigabit transceiver. The HPC carrier does only provide 8 out of 10 MGT lanes.

Eye scans were performed at 4 different lane rates from 2.970 Gbit/s up to 10 Gbit/s.

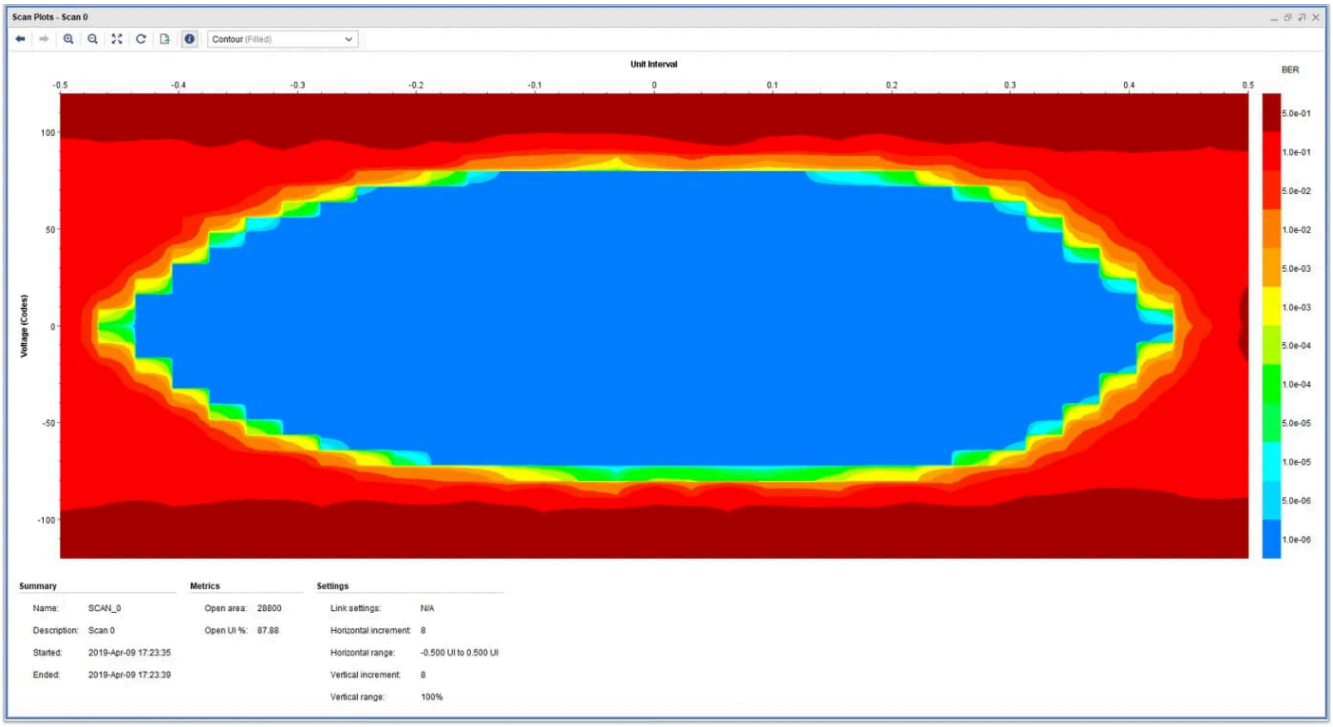


Fig. 12: An Eye-scan with FMC loopback board and Xilinx IBERT core at 2.970 GBit/s MGT lane rate.

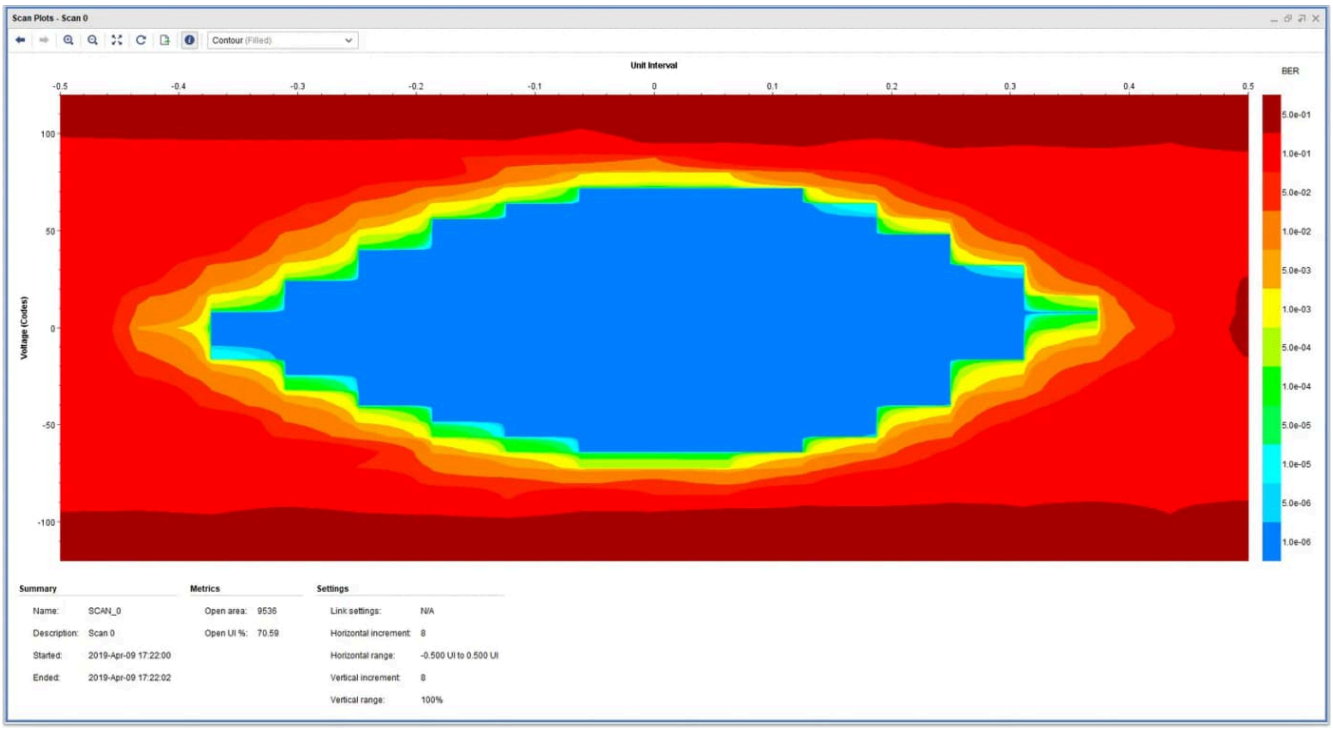


Fig. 13: An Eye-scan with FMC loopback board and Xilinx IBERT core at 5.940 GBit/s MGT lane rate.

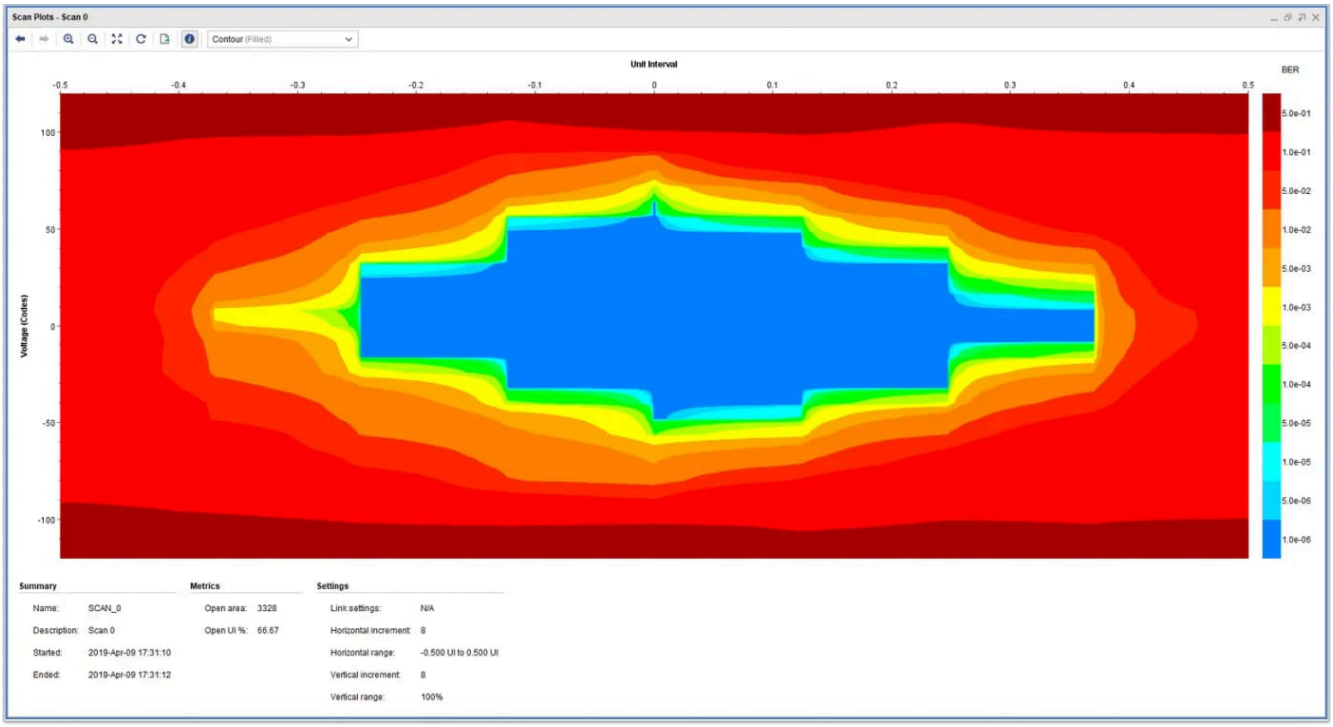


Fig. 14: An Eye-scan with FMC loopback board and Xilinx IBERT core at 8.500 GBit/s MGT lane rate.

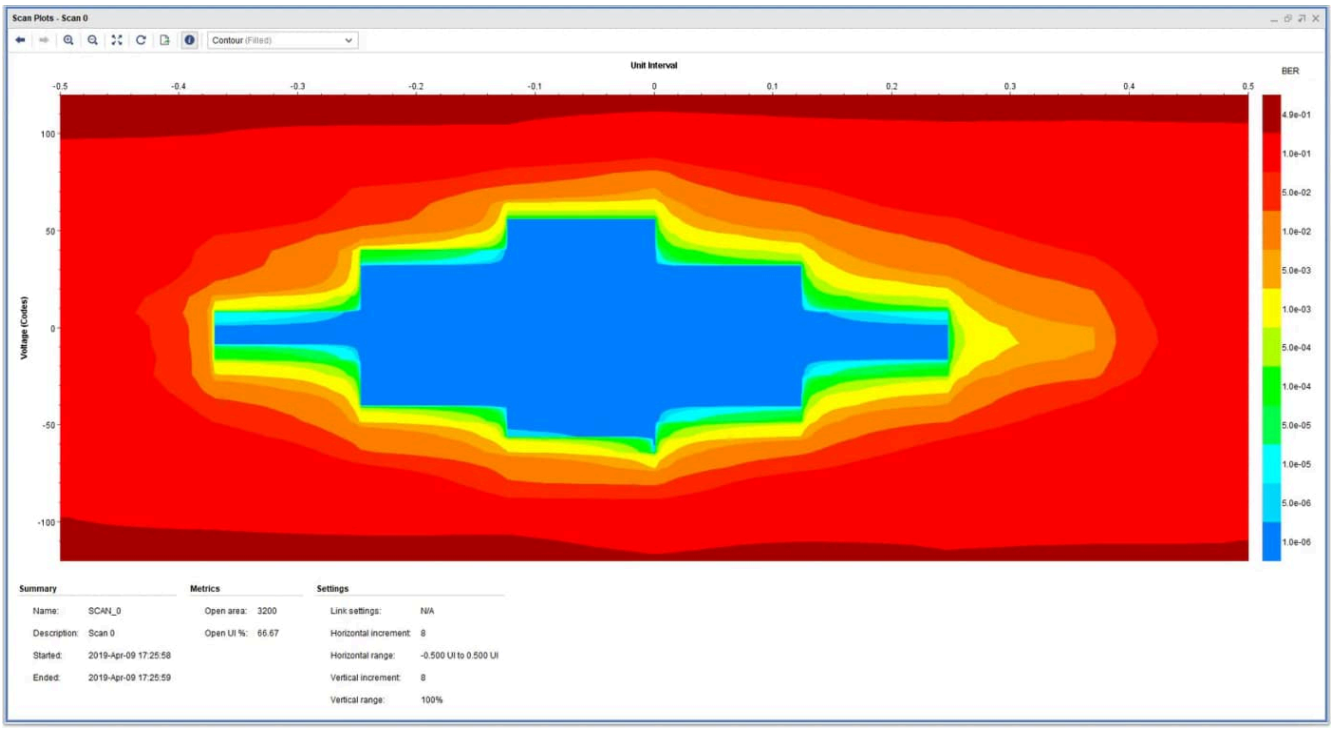


Fig. 15: An Eye-scan with FMC loopback board and Xilinx IBERT core at 10.000 GBit/s MGT lane rate.

2.3 Transceiver loops (DP0 to DP9)

Each transceiver lane is looped on itself: DPn_C2M_P/N is connected to DPn_M2C_P/N (n = 0 .. 9). The loops are plain differential traces. There are no AC coupling capacitors and no other components in the loops. The routed length of each loop is listed in tab. 2.

Coupling. The module does not AC-couple the lanes. Transmitter and receiver of the carrier are therefore connected DC-coupled. Whether this is an allowed operating mode depends on the transceiver of the carrier: check the receiver termination and common-mode settings of your device. Many FPGA transceivers are specified in their default receiver setting only with an external series capacitor.

Data rate. Tested data rates (PRBS-31, carrier: AMD Kintex UltraScale+ GTY, transmitter at default swing, no pre-

or post-cursor, receiver in default DFE mode, no tuning):

Line rate	Result
12.5 Gbit/s	0 errors on all 14 lanes of a two-port carrier (ten-lane port and four-lane port, two modules), 1.7×10^{14} bits per lane (3 h 46 min); repeated in a 4 h run (2.9×10^{15} bits in total over 16 lanes, 0 errors). On a second carrier: 0 errors on the four-lane port, 2.0×10^{13} bits per lane.
12.5 Gbit/s, reference clock from the FPGA	0 errors on all ten lanes of the ten-lane port, 2.0×10^{13} bits per lane. The 125 MHz reference clock was generated in the FPGA of the carrier, driven out on LA01 and LA18 (1.2 V pseudo-differential) and received through the module on GBTCLK0_M2C and GBTCLK1_M2C. The result is the same as with the clock generator of the carrier. The jitter of the clock was not measured.
above 12.5 Gbit/s	Not tested (12.5 Gbit/s is the limit of the transceivers on the test carrier).

Maximum data rate: no limit of the module has been found up to 12.5 Gbit/s. A maximum rate is not specified: the usable rate depends on the carrier lane and on the DC-coupled operating mode.

Recommended use.

- Use the module to check that every transceiver lane of a carrier is connected and carries data (functional test), and as a stress test.
- Do not judge the signal quality of a carrier lane from a result with this module alone.
- Seat the module fully before a transceiver test and re-seat it once before judging a failing lane.

2.4 General information

At this point it is important to mention again that the FMC Loopback module has been optimized for the best price/performance ratio. All results were achieved with a 2 layer PCB with FR-4 material. The signal lanes are not impedance controlled!

The module is passive: no supply rail is needed for any of the loops. Unless the solder jumper is closed, the module does not pull PRSNT_M2C_L low. A carrier that switches the supplies of the port on PRSNT_M2C_L then reports that no module is present and leaves 3P3VAUX off; the loops still work. On the MANZA DUO carrier the PRSNT override switch of the port serves the same purpose as the jumper.

FMC connectors are specified for a limited number of mating cycles. Replace a module that is used as a daily tester when lanes start to drift.

3. Electrical data (pin description)

The printed circuit board is open-source hardware! You can download the FMC Loopback Module schematics and FMC Loopback board layout files in their latest revision from https://iamelectronic.com.

Tab. 1: Bill of materials (BOM) of FMC Loopback Board

Comment	Description	Designator	Manufacturer	Partnumber	Qty
LED green	SMD mono-color Chip LED, WL-SMCW, Green	LED1, ..., LED11	Wuerth Elektronik	150060GS75000	11
MC-HPC-10	MC-HPC-10, FMC High-pin count connector, lead free, 400 I/Os, male, 10 mm mated stack height	P1	Samtec	ASP-134488-01	1
100R	100R 0.1W 5% 0603 (1608 Metric) SMD	R1, ..., R7, R10, R11	Panasonic	ERJ-3GEYJ101V	9
1K8	1K8 0.1W 5% 0603 (1608 Metric) SMD	R8, R9	Yageo	RC0603JR-071K8L	2

A description of the signals from the HPC connector can be found at /knowledge/fmc/pinouts/.

The transceiver loops with their source and destination pins are listed in tab. 2.

Tab. 2: Transceiver loops with their source and destination pins (locations) and the routed length of each loop on the PCB.

	Source		**Destination**	**Loop length**
C6	DP0_M2C_P	C2	DP0_C2M_P	5.6 mm
C7	DP0_M2C_N	C3	DP0_C2M_N	5.6 mm
A2	DP1_M2C_P	A22	DP1_C2M_P	27.0 mm
A3	DP1_M2C_N	A23	DP1_C2M_N	28.0 mm
A6	DP2_M2C_P	A26	DP2_C2M_P	32.2 mm
A7	DP2_M2C_N	A27	DP2_C2M_N	32.3 mm
A10	DP3_M2C_P	A30	DP3_C2M_P	35.9 mm
A11	DP3_M2C_N	A31	DP3_C2M_N	35.0 mm
A14	DP4_M2C_P	A34	DP4_C2M_P	39.8 mm
A15	DP4_M2C_N	A35	DP4_C2M_N	38.9 mm
A18	DP5_M2C_P	A38	DP5_C2M_P	44.4 mm
A19	DP5_M2C_N	A39	DP5_C2M_N	43.4 mm
B16	DP6_M2C_P	B36	DP6_C2M_P	44.7 mm
B17	DP6_M2C_N	B37	DP6_C2M_N	43.8 mm
B12	DP7_M2C_P	B32	DP7_C2M_P	40.6 mm
B13	DP7_M2C_N	B33	DP7_C2M_N	39.5 mm
B8	DP8_M2C_P	B28	DP8_C2M_P	37.0 mm
B9	DP8_M2C_N	B29	DP8_C2M_N	36.2 mm
B4	DP9_M2C_P	B24	DP9_C2M_P	31.8 mm
B5	DP9_M2C_N	B25	DP9_C2M_N	31.8 mm

4. Mechanical data

The board outline is not defined by ANSI/VITA 57.1 standard. It was chosen in such a way that the space requirement is very small. However, the outer dimensions do not exceed the defined outlines of the ANSI/VITA 57.1 FMC standard, so the FMC loopback board should fit on any FMC carrier board. Exact dimensions are given in figure 15.

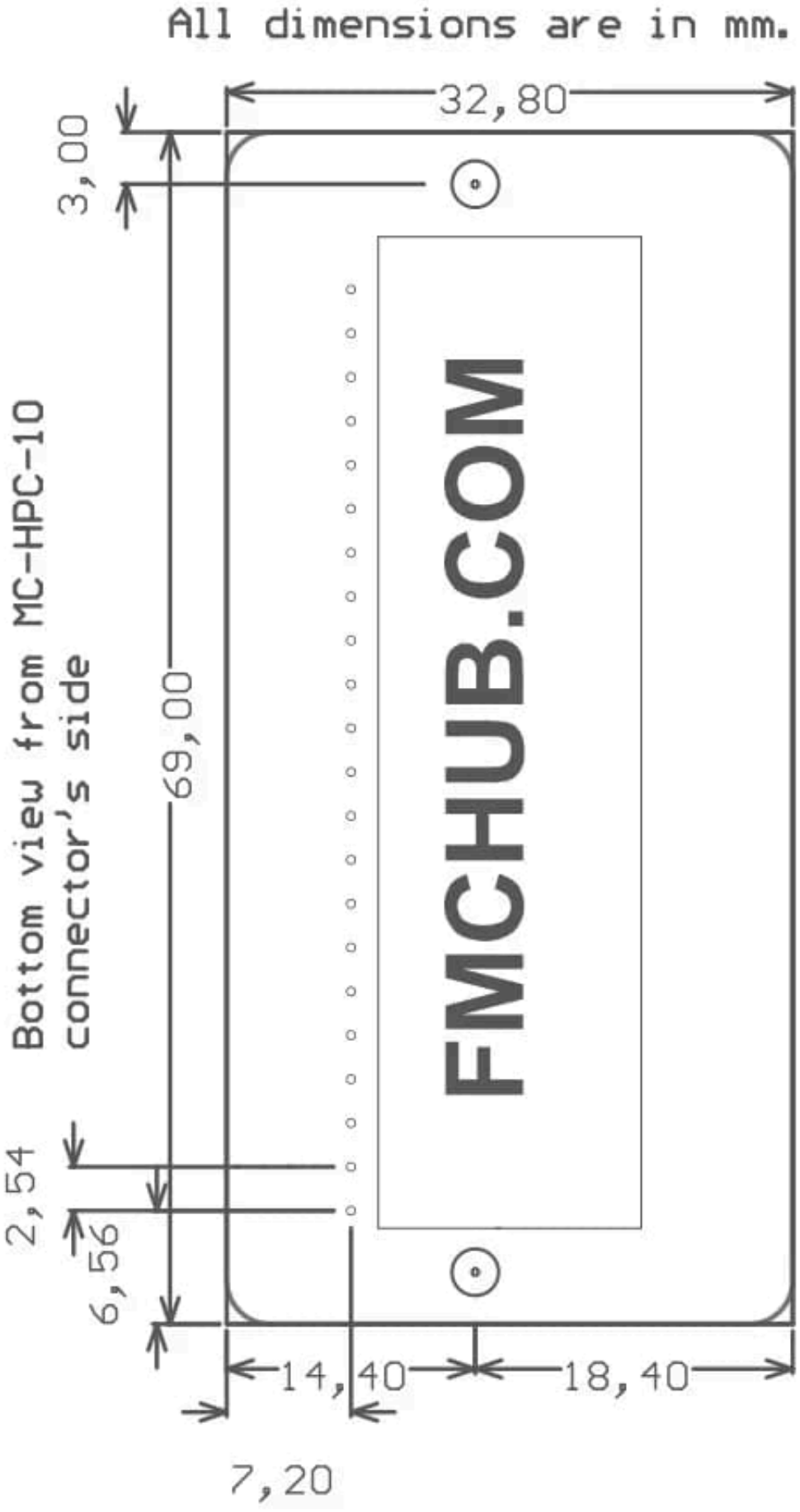


Fig. 16: Mechanical drawing of the FMC Loopback Module.

The mounting holes are plated but have no electrical connection. Their sizes and positions are in accordance with ANSI/VITA 57.1.

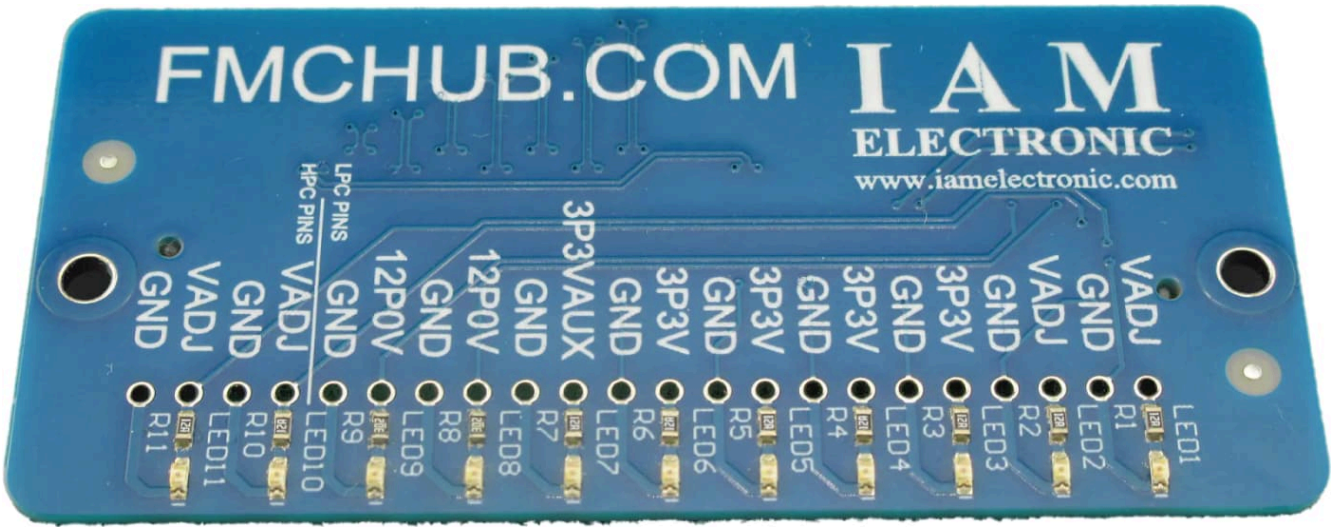


Fig. 17: Product photo of FMC Loopback Module (top view).

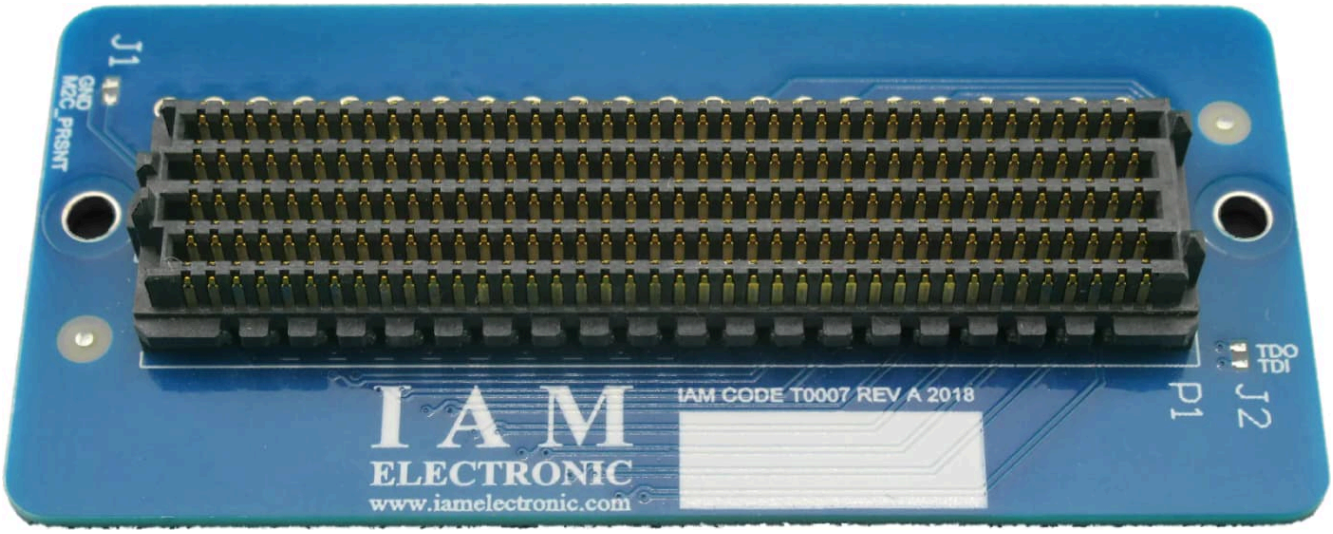


Fig. 18: Product photo of FMC Loopback Module (bottom view).

5. Ordering information

The FMC Loopback Module can be ordered at various online market places, or you can request a quotation by sending an e-mail to info@iamelectronic.com.

Tab. 3: Assembly variants of FMC Loopback Module with product numbers and market places.

Product no.	Description	Market place	Request quote	Standard lead time
T0007	FMC Loopback Module with MC-HPC-10 connectors and green LEDs.	IAM Electronic Shop Ebay #184024624141 Tindie #16652 DigiKey 6068-T0007-ND	info@iamelectronic.com	Normally in stock, otherwise 3 weeks

6. Document history

Document number:

Version history:
2026/11/23: Transceiver loops described (2.3). Loop count, block diagram and tab. 2 corrected. Notes on PRSNT_M2C_L and mating cycles added
2019/04/10: Added links to reference design + minor changes
2019/04/09: Initial release