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FMC HPC Height Extender

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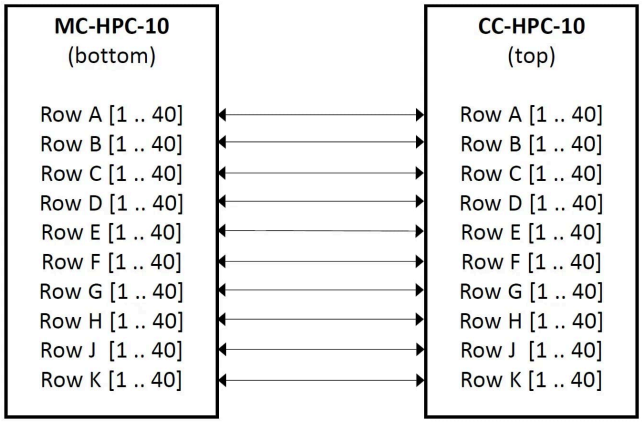
Height Extender Board for FPGA Mezzanine Cards

Features

- VITA 57.1 FMC form-factor height extender card
- Fits LPC and HPC carriers, takes LPC and HPC mezzanines
- HPC mezzanine card connector (MC-HPC-10) on the bottom side
- HPC carrier card connector (CC-HPC-10) on the top side
- Raises the mezzanine by 11.6 mm
- Full 400-pin direct pass-through connectivity
- VADJ and all other rails passed through unchanged
- All 10 transceiver lanes tested from 3.75 to 12.5 Gb/s
- Mates carriers and mezzanines that do not keep to the FMC outline
- Stackable assembly
- Open-source hardware

Block diagram



The photos below show the bottom side with HPC mezzanine card connector (MC-HPC-10) and top side with HPC carrier card connector (CC-HPC-10).

Applications

- Mating oversized mezzanines and non-compliant carriers
- Extending board-to-board spacing for FPGA carrier and mezzanine cards
- Extending lifecycle of FPGA carrier card FMC connectors in test platforms
- Research and education with FPGAs

1. Description

The **FMC HPC Height Extender** increases the vertical spacing between an FPGA carrier card and an FMC mezzanine (*ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard*). It provides an HPC mezzanine card connector (MC-HPC-10) on the bottom side and an HPC carrier card connector (CC-HPC-10) on the top side, and routes all 400 pins directly through. The mezzanine sits 11.6 mm higher: 10 mm stack height plus the 1.6 mm PCB. The extender was developed for carriers and mezzanines that do not keep to the FMC outline. An FMC HPC U.FL Debug Board (T0017), which is wider than a single-width module, did not fit a carrier with an SFP cage next to the FMC connector. Raised by the extender, it could be mated without problems. In the same way, a carrier that places components inside the keep-out regions of the FMC outline can take a standard mezzanine. The extender fits both LPC and HPC carriers and takes both LPC and HPC mezzanines.

2. Application information

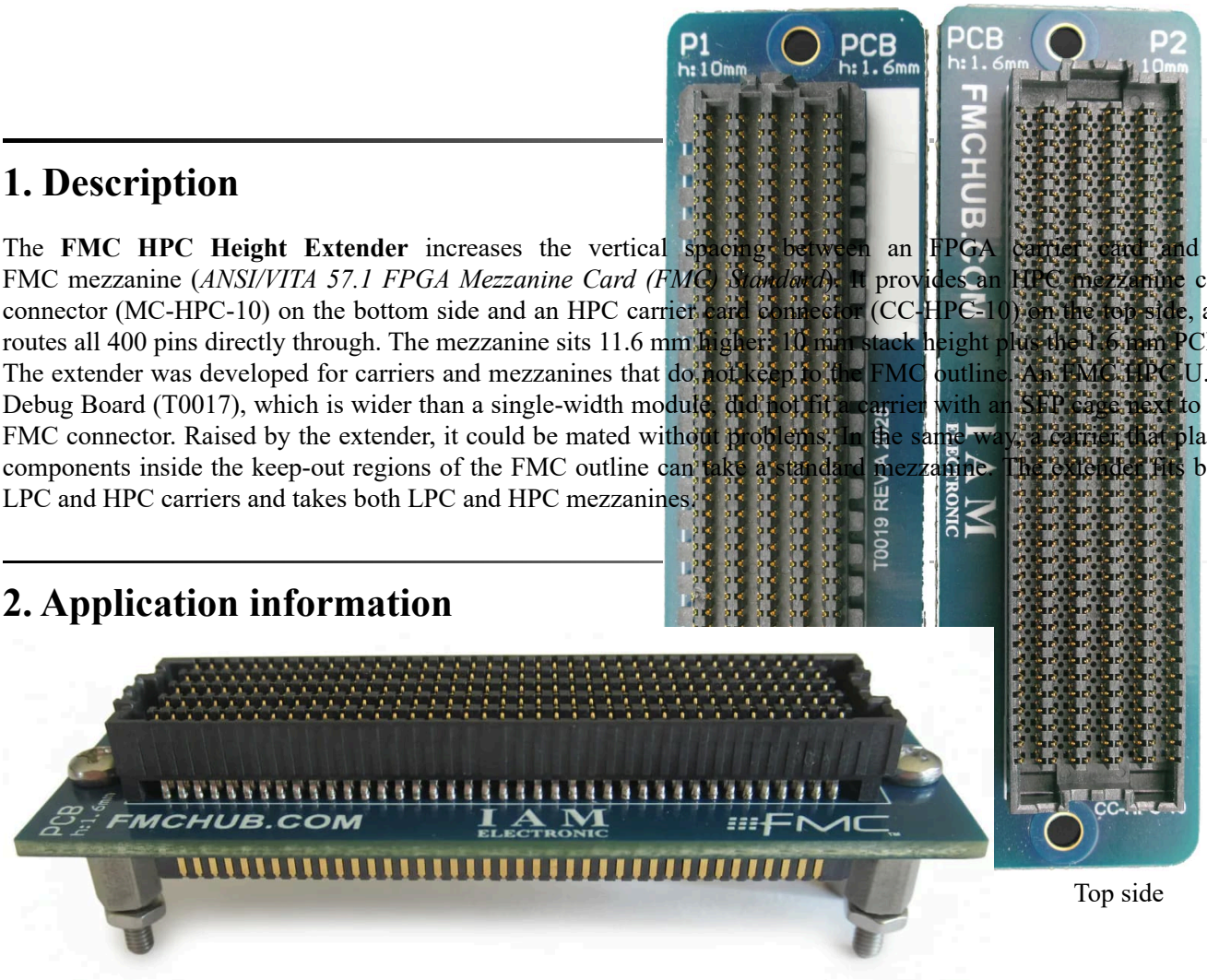


Fig. 1: FMC HPC Height Extender.

2.1 Oversized mezzanines

If an FMC mezzanine exceeds the standard outline, the extender lifts it above parts of the carrier next to the FMC site, such as an SFP cage.

2.2 Carriers with non-compliant layouts

The extender allows the use of carrier boards that place tall components in the keep-out regions of the FMC outline.

2.3 Test platforms

When mezzanines are changed often, the extender takes the mating cycles instead of the FMC connector of the carrier.

3. Electrical data (pin description)

The printed circuit board is open-source hardware! You can download the FMC HPC Height Extender Board schematics and PCB layout files in their latest revision from the GitHub repository. The parts list (see tab. 1) consists of only two parts, both from Samtec.

Tab. 1: Parts list of the FMC Height Extender Board.

FMC connector	Samtec part no.	Description
P2: CC-HPC-10	ASP-134486-01	carrier card connector, top side, high-pin count (HPC), 400 I/O
P1: MC-HPC-10	ASP-134488-01	mezzanine card connector, bottom side, high-pin count (HPC), 400 I/O, 10 mm mated stack height

A description of the signals from the HPC and LPC connector can be found at /knowledge/fmc/pinouts/.

Pin Mapping:
All 400 pins (rows A to K, pins 1 to 40) are routed directly through.

HPC Compatibility:
Provides full 400-pin connectivity.

LPC Compatibility:
The extender fits LPC carriers as well as HPC carriers, and takes low-pin count (LPC) mezzanines. LPC connectors use a defined subset of the HPC pins. Unused pins remain unconnected when operating in LPC mode.

Voltage Support:
VADJ and all other rails are passed through unchanged. The VADJ level is set by the carrier, as without the extender.

PCB Design:
Pass-through only, with via-in-pad design (filled and capped vias) and no other components.

Data Rate Capabilities:
All ten multi-gigabit transceiver lanes DP0 to DP9 have been tested through the height extender at the same time on a prototype of the MANZA DUO carrier (Kintex UltraScale+ XCKU3P, GTY transceivers, FMC port J1), with an XM107 loopback card on top of the extender, AMD IBERT, PRBS-31 and default transceiver settings without tuning (tab. 2). Every lane passes the extender twice on this loop. A bit count N without errors bounds the bit error rate below 3/N with 95 % confidence. 12.5 Gb/s is the highest line rate of the GTY transceivers in the package of this FPGA, so the limit of the extender was not reached.

Tab. 2: Ten lanes through the height extender, MANZA DUO carrier.

Line rate	Lanes	Bits per lane	Errors	BER (95 %)	Eye opening, worst lane
12.5 Gb/s	DP0 to DP9	3.0E12	0	< 1E-12	0.60 UI
10.3125 Gb/s	DP0 to DP9	3.1E12	0	< 1E-12	0.68 UI
8.5 Gb/s	DP0 to DP9	3.1E12	0	< 1E-12	0.54 UI
6.25 Gb/s	DP0 to DP9	3.0E12	0	< 1E-12	0.63 UI
5.0 Gb/s	DP0 to DP9	3.0E12	0	< 1E-12	0.75 UI
3.75 Gb/s	DP0 to DP9	3.0E12	0	< 1E-12	0.81 UI

The eye opening is the horizontal opening at a BER of 1E-6, measured at the FPGA receiver after the complete loop, on one prototype. It does not fall smoothly with the rate: the receiver equaliser adapts per rate, 8.5 Gb/s runs on the second transceiver PLL, and single scans spread by a few percent. Fig. 2 to fig. 7 show the eye scans of lane DP0 at every rate.

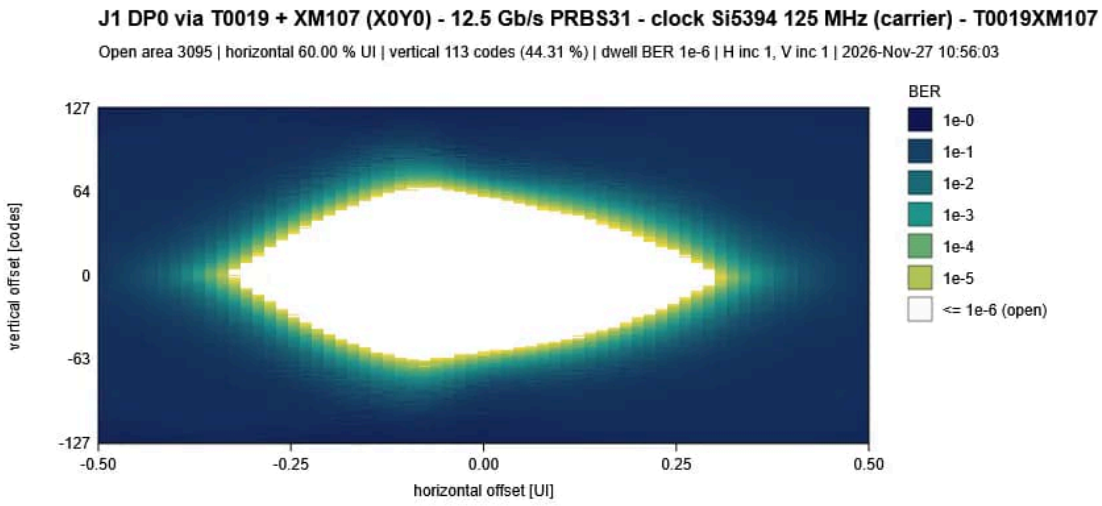


Fig. 2: Eye scan of lane DP0 at 12.5 Gb/s, PRBS-31, through the height extender and an XM107 loopback card.

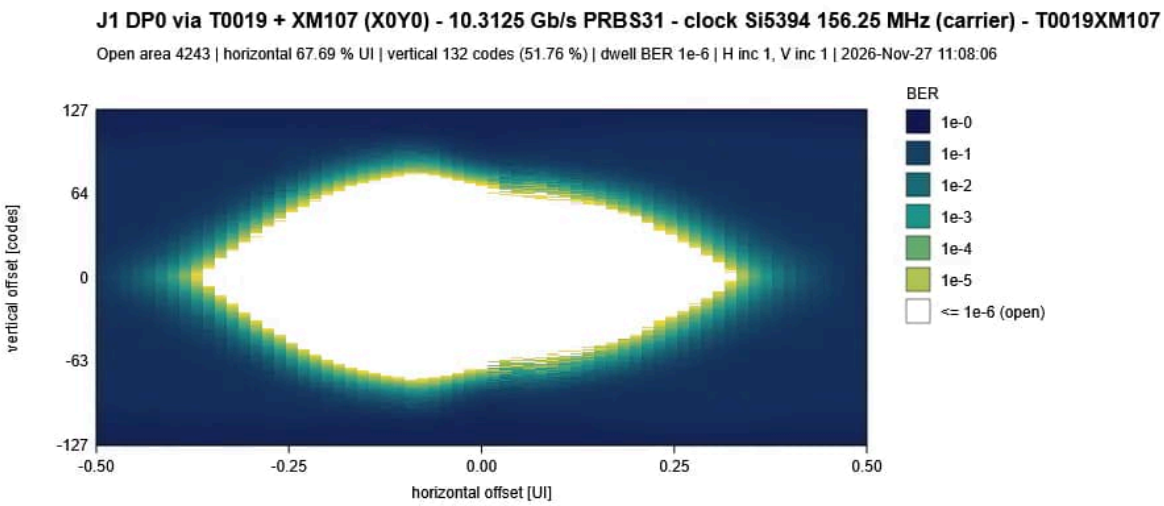


Fig. 3: Eye scan of lane DP0 at 10.3125 Gb/s, PRBS-31, same set-up.

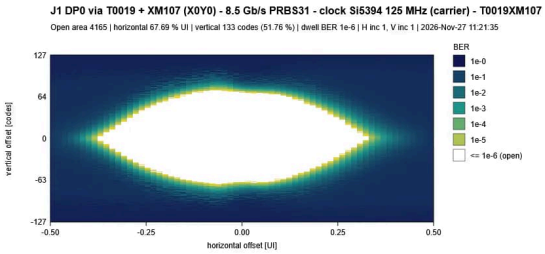


Fig. 4: Lane DP0 at 8.5 Gb/s, PRBS-31.

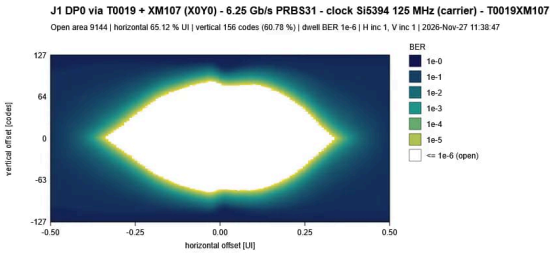


Fig. 5: Lane DP0 at 6.25 Gb/s, PRBS-31.

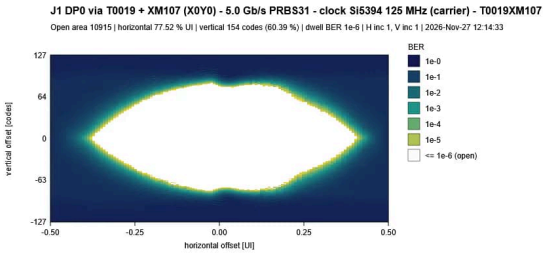


Fig. 6: Lane DP0 at 5.0 Gb/s, PRBS-31.

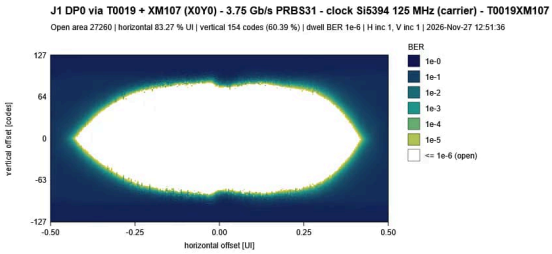


Fig. 7: Lane DP0 at 3.75 Gb/s, PRBS-31.

Earlier, the height extender was tested at 10 Gb/s on eight multi-gigabit transceiver lanes at the same time, with an FMC Loopback Module (T0007) seated on the extender on an Avnet UltraZed-EV carrier card with UltraZed-EV SOM (Zynq UltraScale+ ZU7EV, Xilinx IBERT, PRBS-7). Each lane ran 4.4E14 bits without a bit error, which bounds the bit error rate below 7E-15 with 95 % confidence. Fig. 8 shows the eye diagram, fig. 9 the bit error rate test.

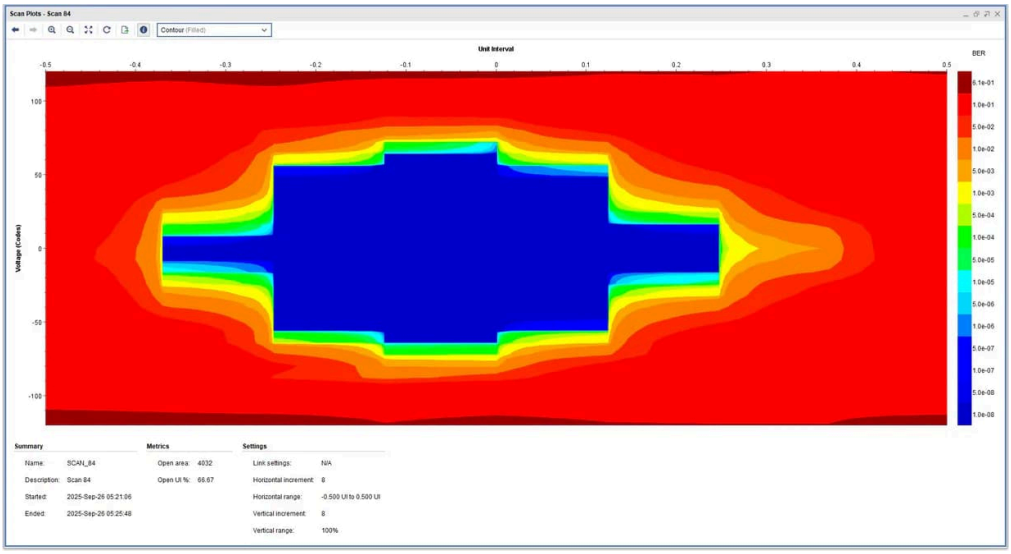


Fig. 8: Eye diagram captured at the FMC loopback at 10 Gb/s.

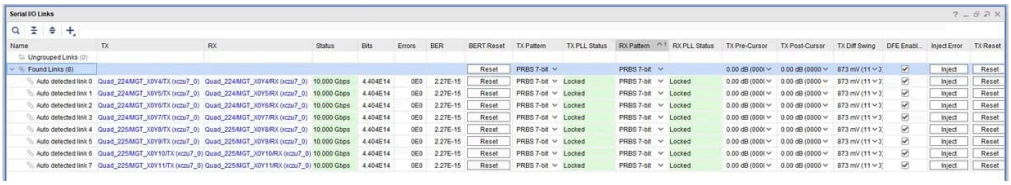
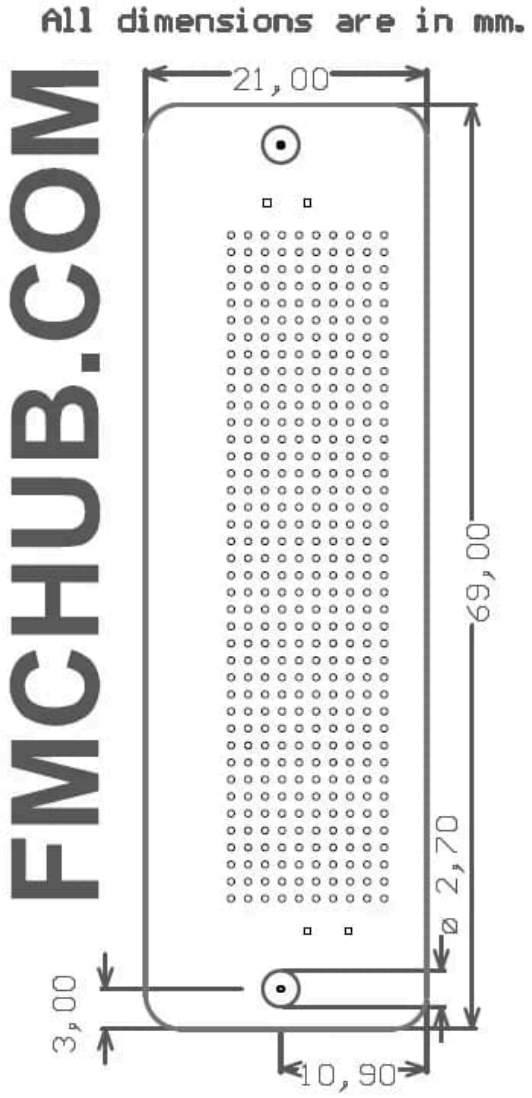


Fig. 9: Bit error rate test of eight lanes at 10 Gb/s: 4.4E14 bits per lane, no errors.

4. Mechanical data

The board lies within the ANSI/VITA 57.1 outline for single-width FMC modules. The board was designed with minimal outline, such that absolute board dimensions are 21.00 mm x 69 mm. Exact dimensions are given in fig. 10.



Symbol	Count	Hole Size	Plated
○	400	0,254mm (10,00mil)	PTH
□	4	1,270mm (50,00mil)	NPTH
✪	2	2,700mm (106,30mil)	PTH
	406 Total		

Fig. 10: Mechanical drawing of the FMC HPC Height Extender Board.

Form Factor:
Within the ANSI/VITA 57.1 single-width FMC module outline

Board Dimensions:
21 mm × 69 mm

Mounting Holes:
Plated, commercial-grade positions per ANSI/VITA 57.1; no electrical connection

Added height:
11.6 mm (10 mm mated stack height plus 1.6 mm PCB). With 10 mm connectors the mezzanine sits 21.6 mm above the carrier instead of 10 mm.

Mounting Kit (included):
Two 10 mm spacers with a threaded stud on one side, two screws and two nuts. They fix the extender on the carrier, and the spacers of the mezzanine screw onto their studs. The spacers of the mezzanine are not included.

Other stack heights:
Custom Samtec connector variants with other stack heights are available. Extenders with them are built on request; please ask for a quotation.

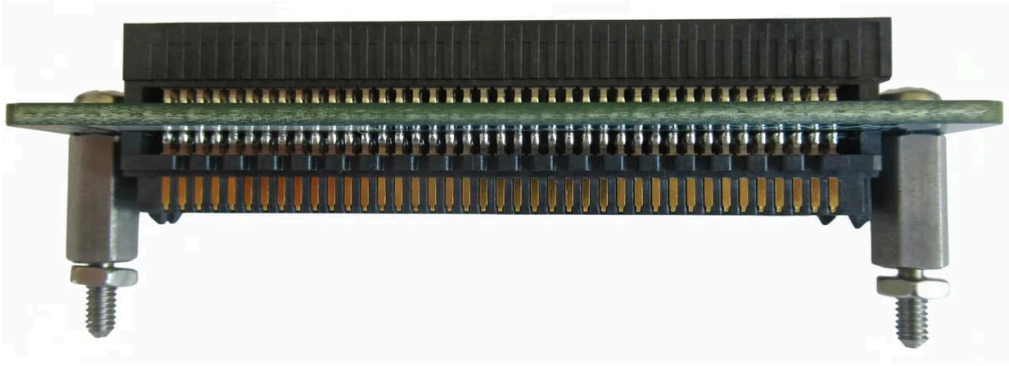


Fig. 11: Side view of the FMC HPC Height Extender board with mounting kit.

5. Ordering information

The FMC HPC Height Extender can be ordered at various online market places, or you can request a quotation by sending an e-mail to info@iamelectronic.com.

Tab. 3: Assembly variants of FMC HPC Height Extender board with product numbers and market places.

Product no.	Description	Market place	Request quote	Standard lead time
T0019	FMC HPC Height Extender Board with both MC-HPC-10 and CC-HPC-10 connectors on bottom and top side.	IAM Electronic Shop Ebay #187570375902 Tindie #39990 DigiKey 6068-T0019-ND	info@iamelectronic.com	Normally in stock, otherwise 6 weeks

6. Document history

Document number:
DS#T0019

Version history:
2026/11/27: Height, dimensions and connector names corrected. Application information rewritten. Ten-lane test from 3.75 to 12.5 Gb/s, mounting kit and other stack heights added
2025/09/26: added eye diagram and BER test
2025/09/15: added links to ordering info section 5
2025/09/09: Initial release