FMC ADC 500M 14b 4cha

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Four-Channel 500 MSPS 14-bit ADC for FMC HPC Carriers, DC-Coupled

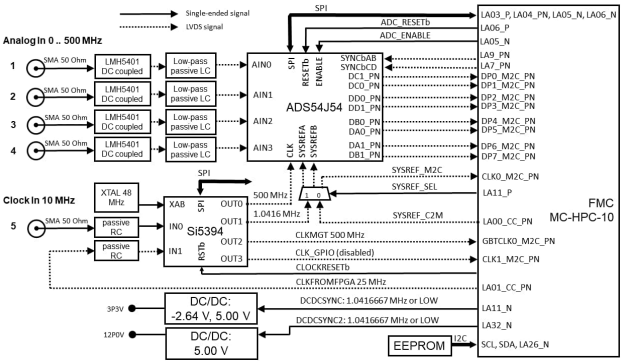
Features

- 4 analog inputs, DC-coupled, single-ended, 50 Ω, SMA
- 500 MSPS, 14 bit, all channels sampled simultaneously (TI ADS54J54)
- Bandwidth DC to 630 MHz (−3 dB), flat within ±0.3 dB up to 550 MHz
- SNR 62.6 dBFS typ. at 5 MHz, 61.5 dBFS typ. at 225 MHz
- ENOB 9.9 bit typ. at 5 MHz, 9.5 bit typ. at 225 MHz
- JESD204B, 8 lanes at 5 Gb/s
- Low-jitter clock tree (Si5394A), lockable to 10 MHz or 25 MHz
- DC/DC converters synchronisable by the FPGA
- FMC HPC, single width, conduction-cooled form factor
- Open hardware (CERN-OHL-S-2.0)

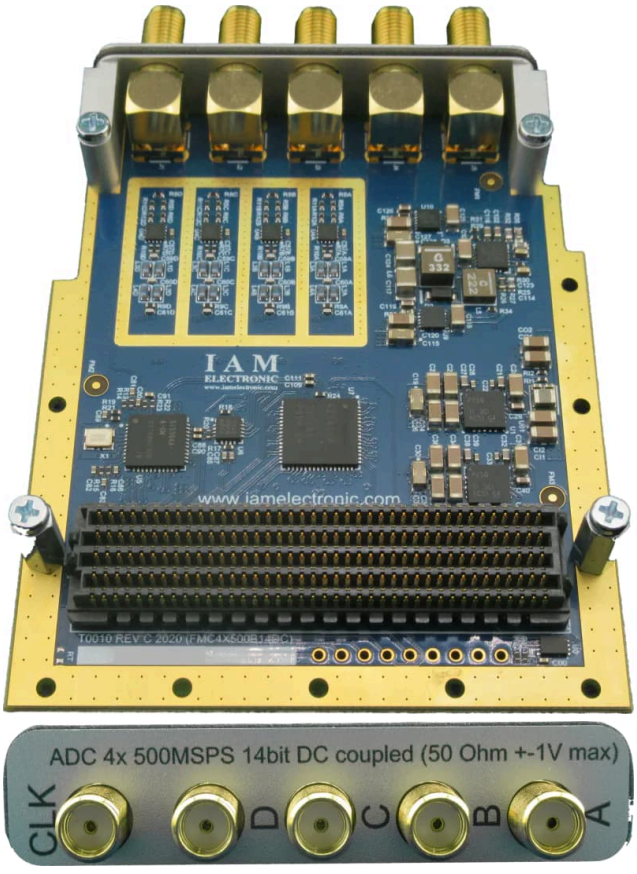
Applications

- Beam instrumentation
- Detector readout and digital pulse processing
- Nuclear electronics
- Scientific instrumentation and high-speed data acquisition
- Test and measurement
- Research and education with FPGAs

Block diagram



The photos below show the top side with the four input stages, the clock generator and the ADC, and the front panel with the clock input and the four analog inputs.



1. Description

The **FMC ADC 500M 14b 4cha** is a four-channel analog-to-digital converter in FPGA Mezzanine Card format (ANSI/VITA 57.1) with a high-pin count (HPC) connector. It samples four DC-coupled, single-ended 50 Ω inputs simultaneously at 500 MSPS with 14 bit resolution and sends the data to the carrier FPGA over JESD204B, eight lanes at 5 Gb/s.

Many high-speed ADC cards in FMC format couple their inputs through transformers or capacitors. That suits RF signals, but it blocks DC and bends slow baseline shifts, and pulse signals from detectors and beam instruments need both: a DC-coupled input and hundreds of MHz of bandwidth. The card was developed for the CERN Beam Instrumentation Group, which procured a series of 60 cards; the renovated beam wire scanners in the PS complex, the SPS and the LHC acquire their signals with it [1]. The design is open hardware under the CERN Open Hardware Licence Version 2, Strongly Reciprocal (CERN-OHL-S-2.0); IAM Electronic GmbH is its commercial producer.

All performance figures in this datasheet are measured at board level, with the DC-coupled front end in the signal path. They are not taken from the data sheet of the ADC.

2. Dynamic performance (measured)

2.1 Series test

Every unit of the series was tested on all four channels at 5 MHz and 225 MHz. Tab. 1 gives the median of these 124 channels (31 units, four channels each) as the typical value, and the value that 90 % of the channels reach or exceed.

Tab. 1: Dynamic performance of the series, 124 channels.

Parameter	f_{in} = 5 MHz, typ.	90 % of channels	f_{in} = 225 MHz, typ.	90 % of channels
SNR	62.6 dBFS	≥ 61.1 dBFS	61.5 dBFS	≥ 60.1 dBFS
ENOB	9.9 bit	≥ 9.6 bit	9.5 bit	≥ 9.4 bit
THD (harmonics 2 to 5)	−78 dBc		−68.5 dBc	
Input level	−1.5 dBFS		−1.9 dBFS	

Fig. 1 and fig. 2 show the spectra of a typical channel of the series, the one whose SNR, ENOB and THD lie closest to the median.

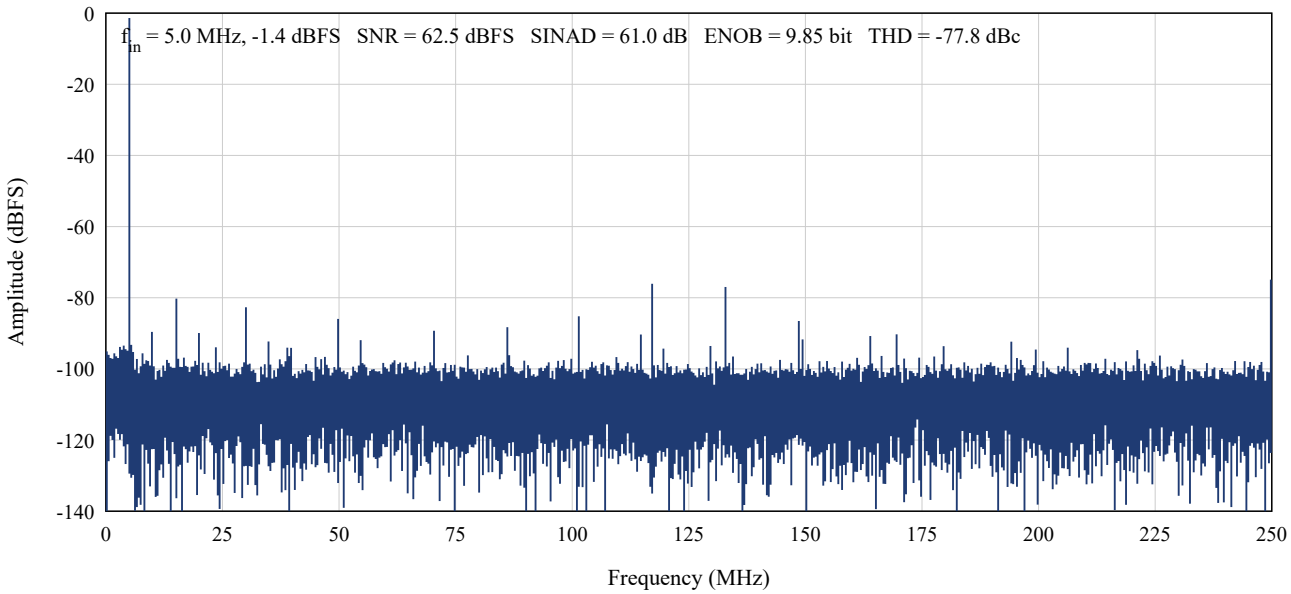


Fig. 1: Spectrum of a typical series channel, 5.0 MHz sine at −1.4 dBFS, 65 536 samples at 500 MSPS.

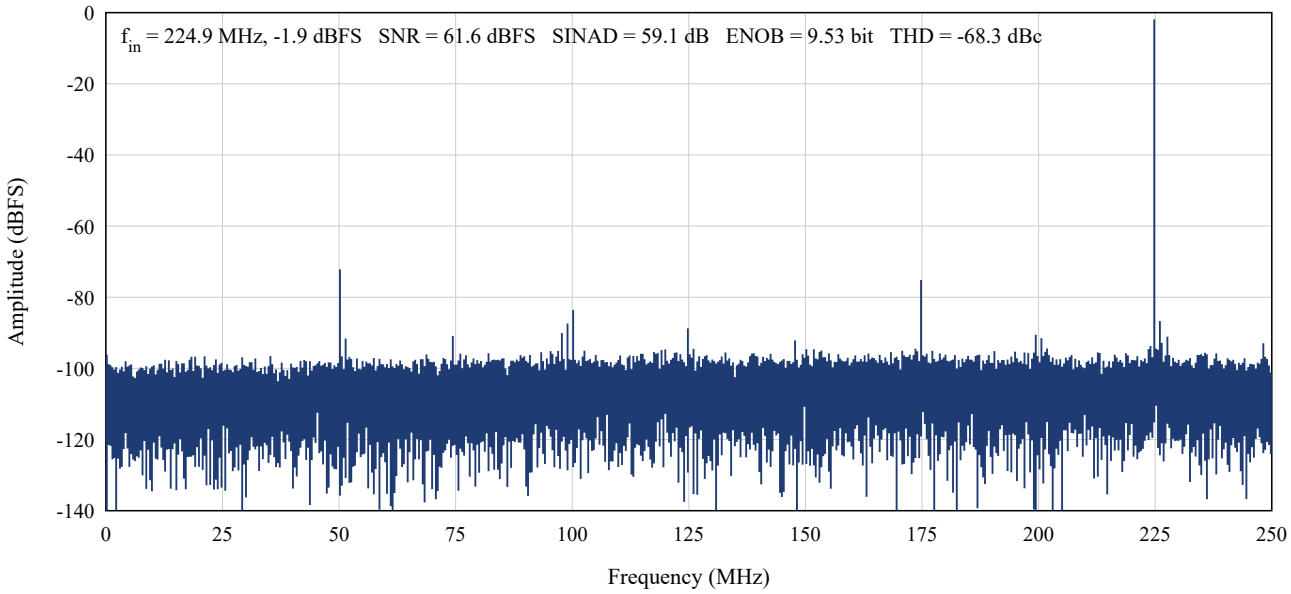


Fig. 2: Spectrum of a typical series channel, 224.9 MHz sine at −1.9 dBFS, 65 536 samples at 500 MSPS.

2.2 Performance across the band

Tab. 2 shows channel A of the prototype from 9 MHz to 249 MHz; fig. 3 to fig. 7 show the spectra of the same records.

Tab. 2: Dynamic performance versus input frequency, channel A.

f_{in}	Input level	SNR	SINAD	ENOB	THD
9.0 MHz	−1.7 dBFS	63.5 dBFS	61.8 dB	9.97 bit	−79.9 dBc
49.0 MHz	−1.2 dBFS	63.1 dBFS	61.7 dB	9.96 bit	−77.6 dBc
88.9 MHz	−1.9 dBFS	63.9 dBFS	61.6 dB	9.94 bit	−72.3 dBc
149.0 MHz	−2.0 dBFS	63.0 dBFS	60.5 dB	9.75 bit	−69.5 dBc
249.1 MHz	−1.6 dBFS	61.7 dBFS	59.4 dB	9.57 bit	−68.0 dBc

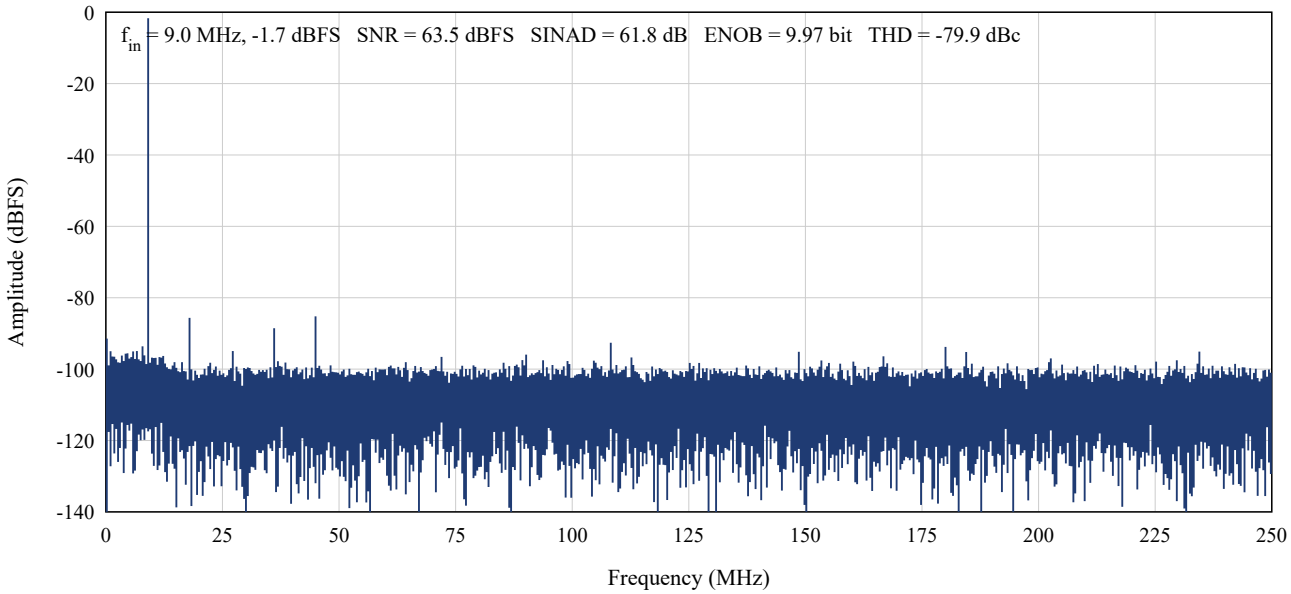


Fig. 3: Spectrum of channel A, 9.0 MHz sine at −1.7 dBFS, 65 536 samples at 500 MSPS.

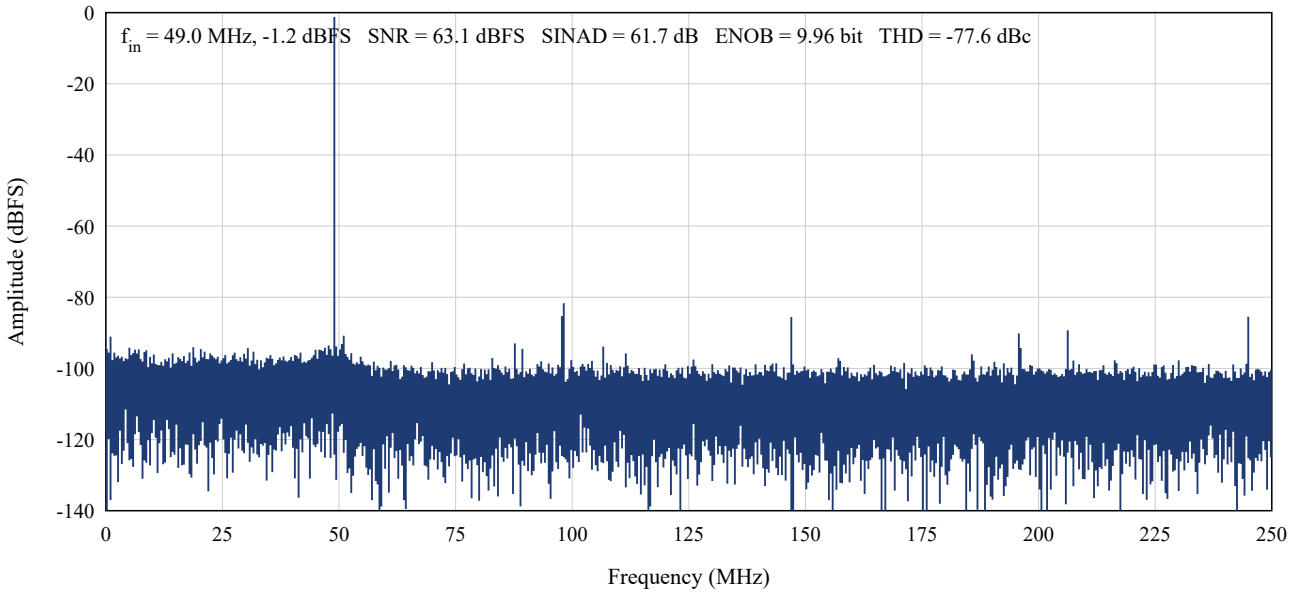


Fig. 4: Spectrum of channel A, 49.0 MHz sine at −1.2 dBFS, 65 536 samples at 500 MSPS.

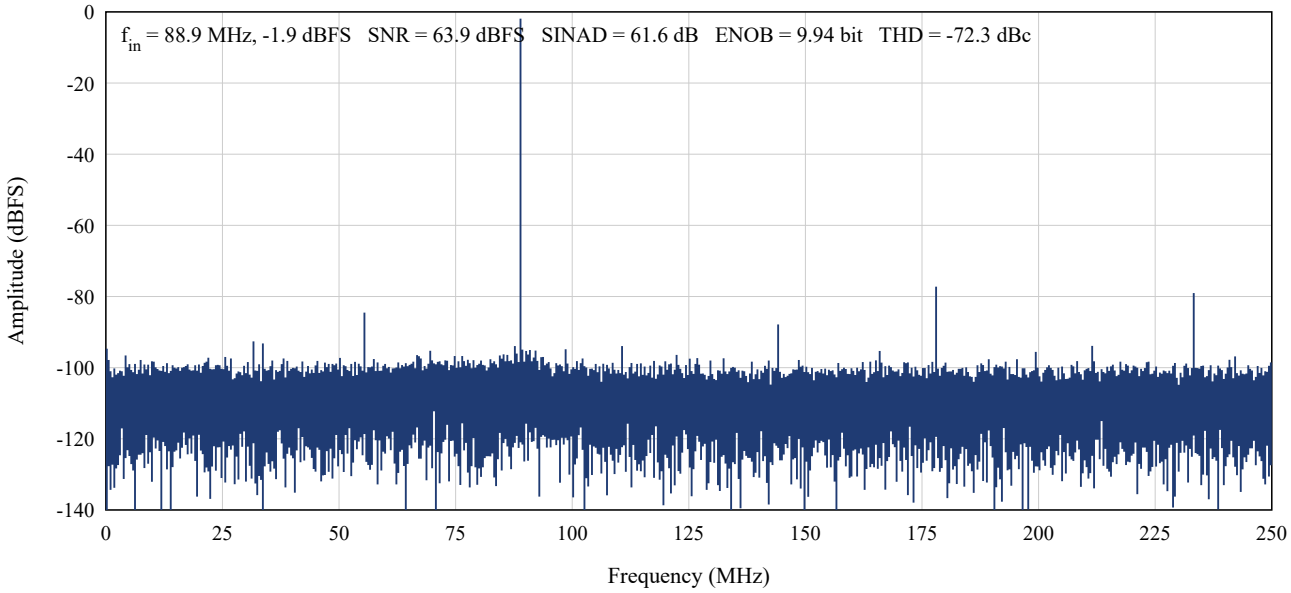


Fig. 5: Spectrum of channel A, 88.9 MHz sine at −1.9 dBFS, 65 536 samples at 500 MSPS.

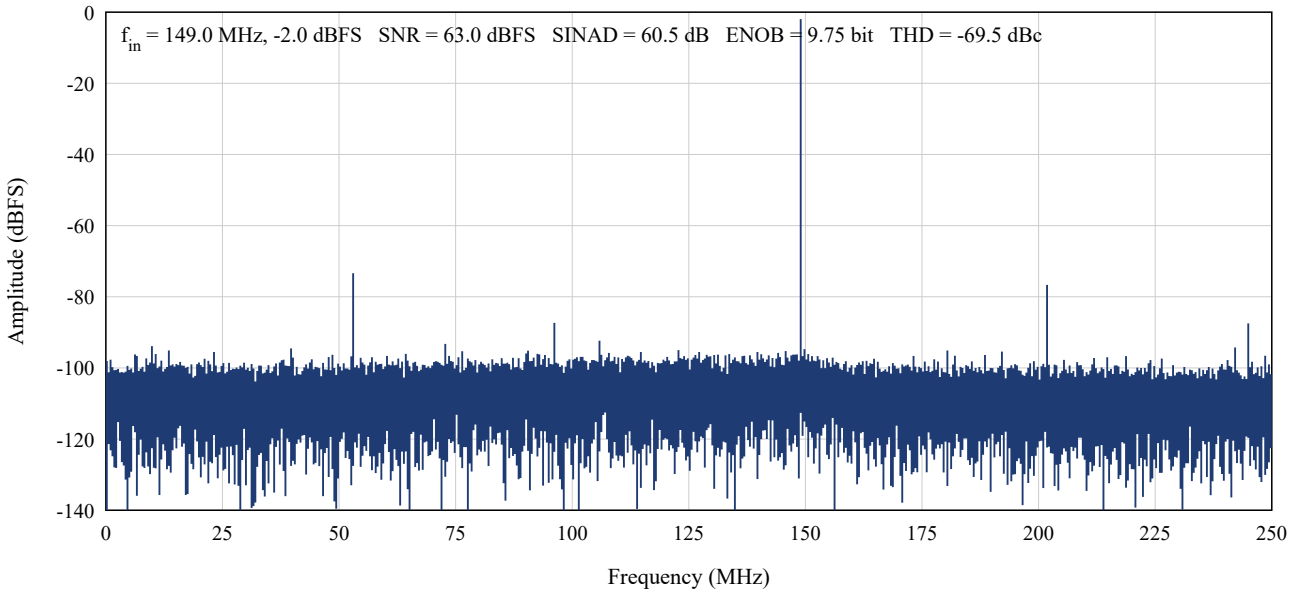


Fig. 6: Spectrum of channel A, 149.0 MHz sine at −2.0 dBFS, 65 536 samples at 500 MSPS.

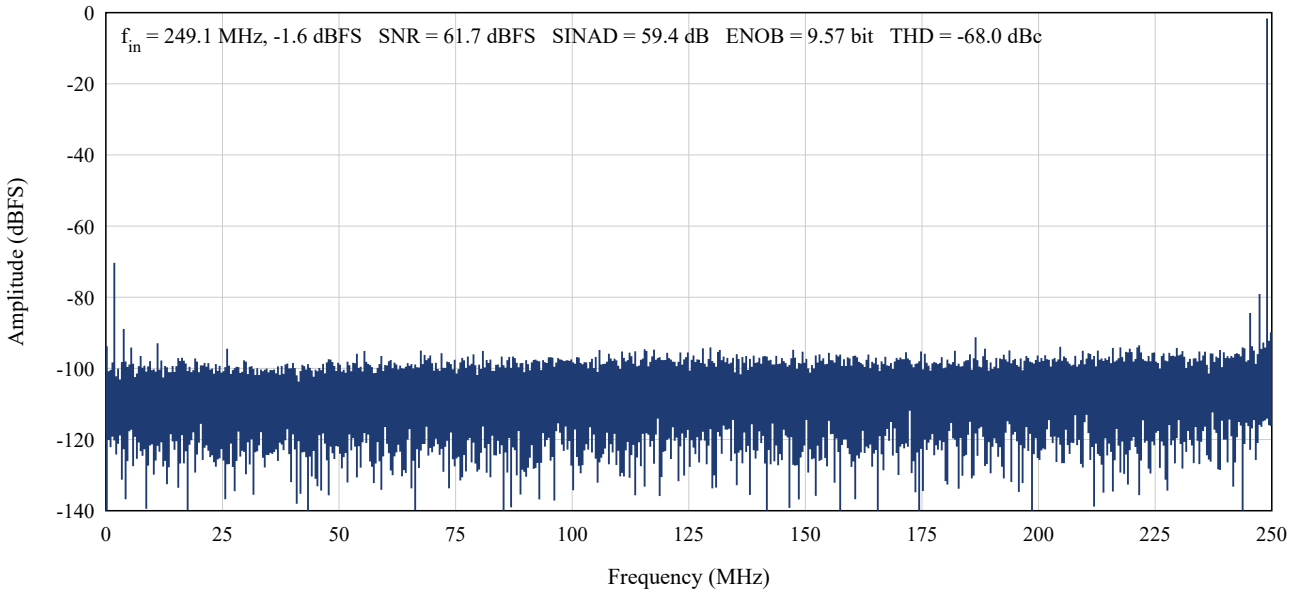


Fig. 7: Spectrum of channel A, 249.1 MHz sine at −1.6 dBFS, 65 536 samples at 500 MSPS.

2.3 Analog input

The front end is flat within ±0.3 dB up to 550 MHz and reaches −3 dB at about 630 MHz (fig. 8). The input impedance stays close to 50 Ω at low frequencies (tab. 3).

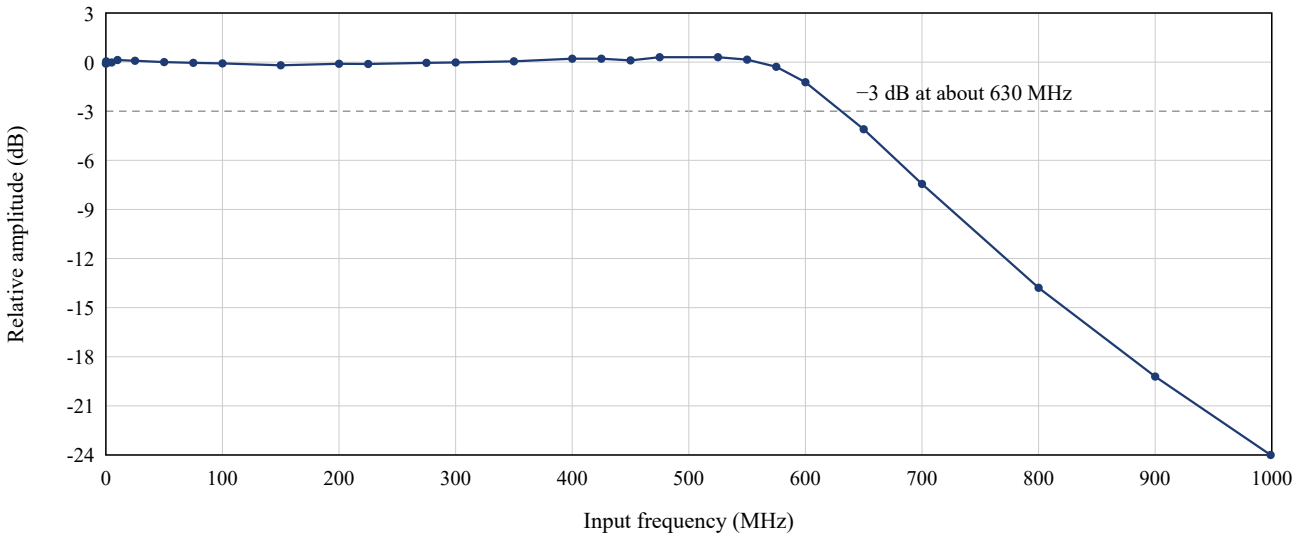


Fig. 8: Frequency response of channel A, relative to the level at 1 to 100 MHz; sine sweep at constant generator level, amplitude from the sine fit.

Tab. 3: Input impedance of channel A.

Frequency	Impedance	VSWR
2 MHz	50.1 Ω + j0.1 Ω	1.00
50 MHz	49.9 Ω − j4.5 Ω	1.09
100 MHz	48.5 Ω − j8.5 Ω	1.19
250 MHz	40.8 Ω − j15.0 Ω	1.47
500 MHz	33.7 Ω − j14.8 Ω	1.70

With the inputs terminated in 50 Ω, the noise of all four channels is below 4 codes rms. Crosstalk at low frequency is better than −85 dB (ramp at 3.8 kHz on channel A, spurs on channel B; the value is limited by the test set-up).

2.4 Test conditions and method

500 MSPS, 65 536 samples per record. Sine from a Rohde & Schwarz SMT02 signal generator through a low-pass filter; generator and card locked by a 10 MHz reference on the clock input. Input level −1.2 to −2.0 dBFS, room temperature about 22 °C. The records are evaluated according to IEEE Std 1241: Nuttall window, four-parameter sine fit, harmonics 2 to 5 fitted and removed. SNR is given relative to full scale (dBFS); SINAD and ENOB are taken from the record as measured. Input impedance measured with a Rohde & Schwarz FPC1500.

The front end stays open from DC to 630 MHz, so it passes its own wideband noise to the converter. The board reaches 61.5 to 62.6 dBFS SNR, where Texas Instruments specifies the ADS54J54 alone at 65.3 dBFS (10 MHz, 500 MSPS) [2]. That is the price of a DC-coupled input with this bandwidth.

A test report for a particular unit, with SNR, SINAD, ENOB and THD of all four channels at typical input frequencies, is available on request at extra charge.

3. Electrical data

The printed circuit board is open-source hardware. Schematics, the Altium PCB project and the manufacturing files are available in the OHWR repository. All signal names and FMC pins below follow the schematics of hardware revision C (2020/02/19).

3.1 Analog inputs and front end

The four inputs are on the front-panel SMA connectors J5 (input 1, ADC channel A), J4 (input 2, channel B), J3 (input 3, channel C) and J2 (input 4, channel D). Each input is terminated with 50 Ω and protected by Schottky diodes to the amplifier supply rails (+4.22 V / −1.02 V). A Texas Instruments LMH5401 fully differential amplifier (gain 2.5) converts the single-ended signal into the differential signal of the ADC; an OPA376 holds the common-mode voltage at the VCM output of the ADC. A 5th-order Chebyshev LC low-pass filter (550 MHz cut-off, gain 0.5) follows. The overall gain from the SMA input to the ADC is 1.25. The inputs are DC-coupled: the DC level of the source is sampled, and there is no offset adjustment on the card. Use a 50 Ω source.

Tab. 4: Analog inputs and ADC.

Parameter	Value
Channels	4, sampled simultaneously
Input type and coupling	Single-ended, DC-coupled, 50 Ω
Full-scale input range	±500 mV
Maximum input signal	±1 V
Bandwidth (−3 dB)	DC to 630 MHz (measured)
Sampling rate, resolution	500 MSPS, 14 bit
ADC	Texas Instruments ADS54J54
Amplifier, filter	LMH5401 (gain 2.5), 5th-order Chebyshev LC low-pass, 550 MHz; overall gain 1.25

3.2 Analog-to-digital converter

The ADS54J54 organises its four channels in two pairs, AB and CD. Each pair forms one JESD204B link with four lanes (L = 4, M = 2, F = 1, K = 32). The eight lanes are AC-coupled (100 nF) and routed to the FMC transceiver pins DP0 to DP7 (tab. 7). The ADC is configured over SPI (chip select SPI_CS0); ADC_RESET and ADC_ENABLE are driven by the FPGA. Its two SYNC~ inputs are LVDS: the FPGA drives them as 1.8 V LVCMOS signals (SYNCbAB on LA09_P, SYNCbCD on LA07_P), which are converted to LVDS on the card. The over-range outputs of the four channels are routed to the FPGA. The ADC has no non-volatile memory; its configuration (section 4.2) must be written after every power-up or reset. Its digital core and I/O supplies are powered from VADJ, which is why VADJ must be 1.8 V.

3.3 Clock generation

All clocks come from a Silicon Labs Si5394A jitter attenuator (85 fs jitter typ.) with a 48 MHz crystal. A working

configuration (tab. 5) is stored in its non-volatile memory, so the card starts up with this clock tree without any programming. A 10 MHz reference on the front-panel SMA J1 (clock input, 50 Ω, AC-coupled), or a 25 MHz LVDS clock from the carrier FPGA on LA01_CC, locks all outputs to the reference. Without a reference the device runs free on its crystal. **Lock the card to the signal source for all ADC performance measurements**, and to a common reference in any multi-card system. The status outputs loss of lock and loss of signal are routed to the FPGA. The output drivers are powered from VADJ, so all clock outputs are 1.8 V LVDS.

Tab. 5: Si5394A clock tree (stored configuration).

Pin	Signal	Frequency	Connection
XA/XB		48 MHz	On-board crystal
IN0	CLKEXT	10 MHz	Front-panel SMA J1, 50 Ω, AC-coupled
IN2	CLKFROMFPGA	25 MHz	LVDS from the FPGA, FMC LA01_CC, 100 Ω, AC-coupled
OUT0	CLKMGT	500 MHz	FMC GBTCLK0_M2C, transceiver reference clock, AC-coupled
OUT1	CLKGPIO	disabled	FMC CLK1_M2C, general-purpose clock
OUT2	SYSREF	1.0416667 MHz	Si53340 SYSREF multiplexer, input CLK1
OUT3	CLKADC	500 MHz	ADS54J54 sample clock

The SYSREF frequency of 1.0416667 MHz equals 500 MHz / 32 / 15: the local multi-frame clock (500 MHz / K) divided by 15, as JESD204B subclass 1 requires with K = 32 and F = 1. Other frequencies can be generated with Silicon Labs ClockBuilder Pro and written over SPI (chip select SPI_CS1) at run time, or stored in the non-volatile memory, which can be written only a limited number of times.

3.4 SYSREF distribution

A Silicon Labs Si53340 LVDS buffer with a 2:1 input multiplexer distributes SYSREF to both ADC links and back to the FPGA (SYSREF_M2C on FMC CLK0_M2C), so the JESD204B receiver uses the same SYSREF as the ADC. The FPGA selects the source with SYSREF_SEL (LA11_P):

Tab. 6: SYSREF source.

SYSREF_SEL	SYSREF source
1	Si5394A OUT2, on-board SYSREF, 1.0416667 MHz, continuous
0	SYSREF_C2M, generated by the carrier FPGA on LA00_CC (LVDS, AC-coupled, 100 Ω)

A SYSREF generated by the FPGA must be derived from the 500 MHz CLKMGT clock domain and meet the SYSREF timing of the ADS54J54.

3.5 FMC signal assignment

The card uses an FMC HPC connector (MC-HPC-10). All single-ended signals are 1.8 V LVCMOS referenced to VADJ. All FMC pins not listed are not connected.

Tab. 7: FMC signal assignment.

FMC pin	Signal	Dir.	Function
DP0_M2C_P/N	DC1	M2C	JESD204B lane, link CD
DP1_M2C_P/N	DC0	M2C	JESD204B lane, link CD
DP2_M2C_P/N	DD0	M2C	JESD204B lane, link CD
DP3_M2C_P/N	DD1	M2C	JESD204B lane, link CD
DP4_M2C_P/N	DB0	M2C	JESD204B lane, link AB
DP5_M2C_P/N	DA0	M2C	JESD204B lane, link AB
DP6_M2C_P/N	DA1	M2C	JESD204B lane, link AB
DP7_M2C_P/N	DB1	M2C	JESD204B lane, link AB
GBTCLK0_M2C_P/N	CLKMGT	M2C	500 MHz transceiver reference clock, LVDS
CLK0_M2C_P/N	SYSREF_M2C	M2C	Selected SYSREF to the FPGA, LVDS
CLK1_M2C_P/N	CLKGPIO	M2C	Si5394A OUT1, disabled in the stored configuration
LA00_P_CC / LA00_N_CC	SYSREF_C2M	C2M	SYSREF from the FPGA, LVDS
LA01_N_CC / LA01_P_CC	CLKFROMFPGA	C2M	25 MHz from the FPGA, LVDS; P is on LA01_N_CC, N on LA01_P_CC
LA02_P	LossLockb	M2C	Si5394A loss of lock, active low
LA02_N	LossSignalb	M2C	Si5394A loss of signal, active low
LA03_P	SPI_CS1	C2M	SPI chip select Si5394A, active low
LA03_N	CLOCKRESET	C2M	Si5394A reset, active low
LA04_P	SPI_MOSI	C2M	SPI data to ADC and Si5394A
LA04_N	SPI_CLK	C2M	SPI clock to ADC and Si5394A
LA05_P	ADC_ENABLE	C2M	ADC enable
LA05_N	SPI_MISO	M2C	SPI data from ADC and Si5394A
LA06_P	ADC_RESET	C2M	ADC reset, active low
LA06_N	SPI_CS0	C2M	SPI chip select ADC, active low
LA07_P	SYNCbCD	C2M	JESD204B SYNC~, link CD
LA08_P / LA08_N	ADC_OVRC / ADC_OVRD	M2C	ADC over-range, channels C and D
LA09_P	SYNCbAB	C2M	JESD204B SYNC~, link AB
LA10_P / LA10_N	ADC_OVRB / ADC_OVRA	M2C	ADC over-range, channels B and A
LA11_P	SYSREF_SEL	C2M	SYSREF source (tab. 6)
LA11_N	DCDCSYNC	C2M	Sync input of the ADP5071 DC/DC converter (tab. 8)
LA32_N	DCDCSYNC2	C2M	Sync input of the LMZM23601 DC/DC converter (tab. 8)
LA33_N, LA33_P, LA31_N, LA31_P, LA29_N	LED1 to LED5	C2M	User LEDs, active high
SCL, SDA	I2C	both	FMC EEPROM, 3.3 V, pull-ups to 3P3VAUX
GA0, GA1		C2M	EEPROM address inputs A1, A0
PRSNT_M2C_L		M2C	Tied to GND (mezzanine present)
12P0V, 3P3V, 3P3VAUX, VADJ		C2M	Supply rails; VADJ = 1.8 V

Lane order and P/N polarity of the DP lanes depend on the routing of the carrier and must be set in the FPGA transceiver configuration.

3.6 Power supply

The card is powered from the FMC rails 12P0V, 3P3V, 3P3VAUX and VADJ. Low-noise LDOs follow the DC/DC converters: 12P0V feeds an LMZM23601 step-down converter and a TPS7A4700 LDO for the 3.3 V analog supply of the ADC and the clock generator; 3P3V feeds an ADP5071 dual converter and LT3045 / LT3094 LDOs for the ±rails of the front end (+4.22 V / −1.02 V), and a TPS7A4700 LDO for the 1.8 V analog supply; VADJ supplies the digital parts of the ADC, the clock outputs and the level shifters through a TPS22970 protection switch, which

opens if VADJ exceeds about 2.1 V; 3P3VAUX supplies the FMC EEPROM. The power LED lights when VADJ is present.

The switching frequency of both DC/DC converters can be synchronised by the FPGA. Driving both inputs with the 1.0416667 MHz SYSREF clock keeps the switching noise coherent with the SYSREF period. Do not leave these inputs floating.

Tab. 8: DC/DC synchronisation inputs.

Signal	Converter	LOW	HIGH	External clock
DCDCSYNC (LA11_N)	ADP5071 (3.3 V input)	internal 1.2 MHz		1.0 to 2.6 MHz
DCDCSYNC2 (LA32_N)	LMZM23601 (12 V input)	auto PFM mode	forced PWM, internal 1 MHz	0.7 to 1.1 MHz

Tab. 9: Supply currents, series test (typ.).

Rail	Current	Power
12P0V	0.29 A	3.5 W
3P3V	1.39 A	4.6 W
VADJ (1.8 V)	0.84 A	1.5 W
Total		**9.5 W**

At 9.5 W the card needs airflow or conduction cooling; do not operate it in a closed enclosure without a defined thermal path.

3.7 FMC FRU EEPROM and LEDs

A 24LC64 I2C EEPROM, powered from 3P3VAUX with 4K7 pull-ups on SCL and SDA, stores the FRU record according to ANSI/VITA 57.1: manufacturer, product name, serial number and the VADJ requirement of 1.8 V. Its address is 0b10101 GA0 GA1 (0x54 to 0x57, set by the carrier). The write-protect pin is tied low, so the record can be rewritten. Five green user LEDs are switched by the FPGA (high = on); a sixth LED shows that VADJ is present.

4. Configuration and bring-up

4.1 Carrier requirements and FPGA control signals

The carrier needs an FMC HPC connector (the card does not fit LPC-only carriers), VADJ = 1.8 V with at least 1 A, at least 1.5 A on 3P3V and 0.4 A on 12P0V, eight FPGA transceivers on DP0 to DP7 for at least 5 Gb/s, GBTCLK0_M2C on a transceiver reference-clock input, LVDS-capable user I/O for LA00_CC and LA01_CC, and CLK0_M2C on a clock-capable input. The FPGA design must drive the following signals:

Tab. 10: FPGA control and status signals.

Signal	FMC pin	Required state
CLOCKRESET	LA03_N	High; pulse low to reset the clock generator
ADC_RESET	LA06_P	High; pulse low to reset the ADC
ADC_ENABLE	LA05_P	High
SYSREF_SEL	LA11_P	1 = on-board SYSREF, 0 = SYSREF_C2M from the FPGA
DCDCSYNC	LA11_N	1.0416667 MHz clock or LOW
DCDCSYNC2	LA32_N	1.0416667 MHz clock, LOW or HIGH
SYNCbAB, SYNCbCD	LA09_P, LA07_P	Driven by the JESD204B receivers, active low
SPI_CS0, SPI_CS1	LA06_N, LA03_P	High except during SPI transfers
SPI_CLK, SPI_MOSI, SPI_MISO	LA04_N, LA04_P, LA05_N	Shared SPI bus
LED1 to LED5	LA33_N, LA33_P, LA31_N, LA31_P, LA29_N	Optional, high = LED on
LossLockb, LossSignalb	LA02_P, LA02_N	Inputs: clock status, active low
ADC_OVRA to ADC_OVRD	LA10_N, LA10_P, LA08_P, LA08_N	Inputs: over-range per channel

4.2 ADC register sequence

The ADC is written over SPI: SPI_CS0 low, R/W bit = 0, 7-bit address, 16-bit data latched on the rising edge of SPI_CLK, SPI_CS0 high. The sequence of tab. 11 sets up 500 MSPS operation with the JESD204B parameters of tab. 12. Keep the order of the writes.

Tab. 11: ADS54J54 register sequence (address / data).

No.	Addr.	Data	Remark	No.	Addr.	Data	Remark
1	0x00	0x8000	4-wire SPI	20	0x1A	0x0020	High-density mode, link CD
2	0x0D	0x0000	JESD reset and init 0	21	0x1D	0x0000	Normal data (tab. 13)
3	0x0D	0x0202	JESD init 1	22	0x1E	0x0000	
4	0x0D	0x0303	JESD reset 1	23	0x1F	0xFFFF	
5	0x01	0xAF7A		24	0x20	0x0000	PRBS off
6	0x02	0x0000		25	0x21	0x2000	
7	0x03	0x4040	Clock divider	26	0x44	0x0074	
8	0x04	0x000F	SYNCbAB, SYNCbCD enabled	27	0x47	0x0074	
9	0x05	0x0000		28	0x4C	0x4000	
10	0x06	0xFFFF		29	0x50	0x0800	
11	0x07	0x0144	Clock switch AB	30	0x51	0x0074	
12	0x08	0x0144	Clock switch CD	31	0x54	0x0074	
13	0x0C	0x31E4	Skip one SYSREF pulse, then use all	32	0x59	0x4000	
14	0x0E	0x00FF	All lanes enabled	33	0x5D	0x0800	
15	0x0F	0x0001	Link AB: F = 1, M = 2	34	0x0D	0x0202	JESD reset 0, init 1
16	0x10	0x03E3	Link AB: K = 32, L = 4	35	0x0D	0x0303	JESD reset 1, init 1
17	0x13	0x0020	High-density mode, link AB	36			Wait two SYSREF cycles (≥ 1.6 µs)
18	0x16	0x0001	Link CD: F = 1, M = 2	37	0x0D	0x0101	JESD reset 1, init 0
19	0x17	0x03E3	Link CD: K = 32, L = 4				

4.3 JESD204B link

Tab. 12: JESD204B parameters.

Link	Channels	L	M	F	K	Lane rate
AB	A, B	4	2	1	32	5 Gb/s
CD	C, D	4	2	1	32	5 Gb/s

Lane rate = 500 MHz × 10/8 (8b/10b) × 16 bit × 0.5 = 5 Gb/s; each 14-bit sample travels in a 16-bit word on two lanes per converter. Bring-up: set CLOCKRESET high and check that the 500 MHz CLKMGT clock is present and the transceiver PLLs lock; configure the receiver with L = 4, M = 2, F = 1, K = 32, 8b/10b, subclass 1; select the SYSREF source and connect SYSREF_M2C to the receiver; set ADC_RESET and ADC_ENABLE high and write tab. 11; assert SYNC~ until the receiver has code-group sync, then check the ILAS and the alignment. A test pattern (tab. 13) verifies the data path independent of the analog inputs. JESD204B/C receiver IP cores for AMD FPGAs are available from IAM Electronic [3].

Tab. 13: Test patterns, register 0x1D.

Value	Output
0x0000	Normal ADC data
0x0060	Ramp
0x0068	Checkerboard (0x1555 / 0x2AAA)

The card runs in production on the CERN VFC-HD carrier (VME64x, Intel Arria V, one FMC HPC site). Any ANSI/VITA 57.1 HPC carrier that meets section 4.1 can be used.

5. Mechanical data

The card follows the ANSI/VITA 57.1 outline for single-width FMC modules in the ruggedized, conduction-cooled form factor, with thermal interfaces for conduction cooling. Mounting holes according to ANSI/VITA 57.1: 2.7 mm for commercial-grade carriers (M2.5 screws), 2.2 mm for ruggedized carriers. The front panel carries the clock input J1 and the four analog inputs J2 to J5. FMC modules are not hot-pluggable: switch off the carrier before inserting or removing the card, and check that the carrier sets VADJ to 1.8 V before the first power-up.

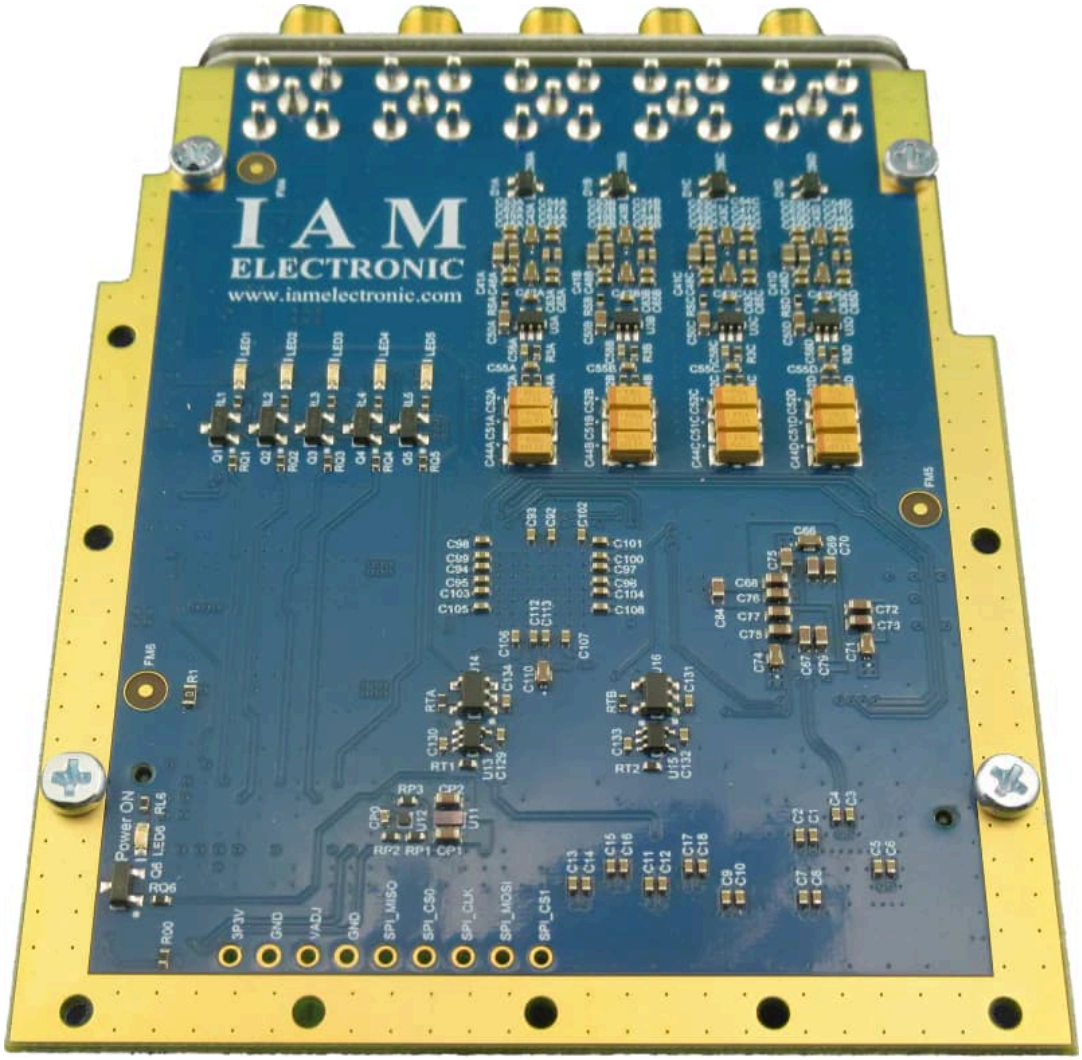


Fig. 9: Bottom side with the LEDs and the test points for 3P3V, VADJ and the SPI lines.

6. Ordering information

The FMC ADC 500M 14b 4cha can be ordered in the IAM Electronic shop and at DigiKey, or you can request a quotation by sending an e-mail to info@iamelectronic.com.

Tab. 14: Product number and ordering.

Product no.	Description	Market place	Request quote	Standard lead time
T0010	FMC ADC 500M 14b 4cha, four channels, 500 MSPS, 14 bit, DC-coupled, FMC HPC, hardware Rev. C. Test report per unit on request, at extra charge.	IAM Electronic Shop DigiKey 6068-T0010-ND	info@iamelectronic.com	Normally in stock, otherwise 10 weeks

7. Resources

[1] D. Belohrad et al., The digital signal processing chain of the CERN LIU BWS, IBIC 2023, TUP044: doi:10.18429/JACoW-IBIC2023-TUP044
[2] Texas Instruments, ADS54J54 data sheet: ads54j54.pdf
[3] JESD204B/C FPGA IP Core: IAM Electronic
[4] OHWR repository (schematics, Altium project, manufacturing files): gitlab.com/ohwr/project/fmc-adc-500m14b4cha
[5] Schematics: fmc-adc-500m14b4cha_schematics.pdf
[6] Silicon Labs Si5395/94/92 data sheet: si5395-94-92-a-datasheet.pdf

8. Document history

Document number:
DS#T0010

Version history:
2026/11/27: Initial release

Hardware history:
2019/07/12: Project start
2019/11/25: First prototype
2020/02/19: Hardware revision C
2021/01/12: 60 cards delivered to CERN
2021/04/01: Design released under CERN-OHL-S-2.0