Tiny 5 × 5 cm FPGA module with Xilinx Artix-7

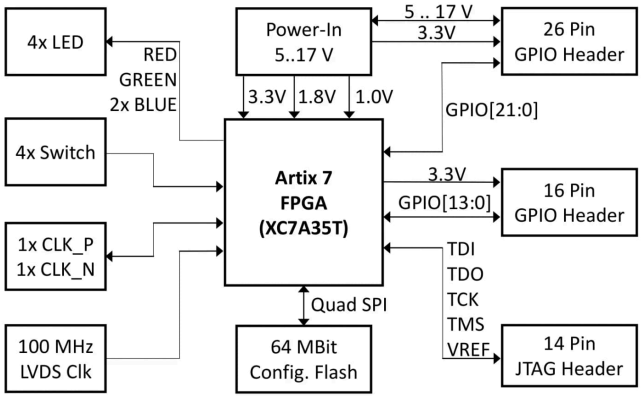
Features

- Dimensions of 5 cm x 5 cm
- 36 User In-/Outputs (10 analog inputs)
- 4 user LEDs
- 4 user Switches
- Optional clock IO with MMCX jacks
- Input voltage range from 5 V to 17 V
- 100 MHz onboard clock
- 64 Mbit configuration memory
- Standard Xilinx JTAG header (14 pin)
- All GPIOs are directly accessible through 2.54 mm pin headers
- Out-of-the-box functionality, no mother- or carrierboard required

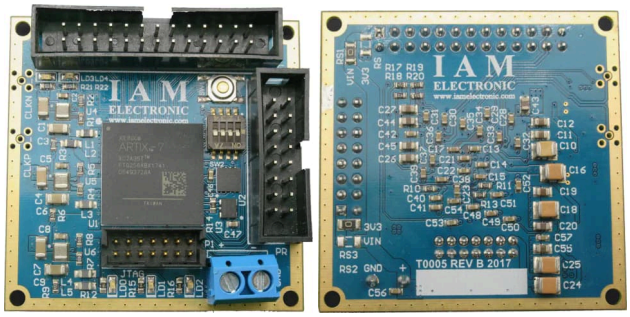
Applications

- Industrial measurements and control
- Digital signal processing
- Interface adaptation
- Easy prototyping
- Education and research with FPGAs

Block diagram



The photos below show both sides of the Artix-7 FPGA Module (equipped with Xilinx XC7A35T-1FTG256C). By default, the board is **not** populated with the two optional MMCX jacks for differential clocking (Input or Output).



Top side Bottom side

1. Description

The **tiny Artix-7 FPGA Module** is an out-of-the-box feature FPGA board with only 5 cm x 5 cm dimensions. It is ready for use by simply connecting a power supply and programming the FPGA or the 64 Mbit SPI flash via the standard Xilinx JTAG connector. The board operates with a wide input voltage range from 5 V up to 17 VDC sourced either by the screw terminal or pin 1 from the PT header (26 pos. male header). The module provides 36 general purpose IOs (GPIOs) through two easily accessible pin headers. Some of the inputs can be used for analog-to-digital conversion with a sample rate of up to 1 MSPS and a resolution of 12 bit (built-in Xilinx XADC module). For connecting auxiliary modules to the connectors, the board includes hardware-selectable power pins. Further, the tiny FPGA module has four programmable LEDs (one green and one red LED, two blue LEDs) and four micro switches for user interactions. On the board is a stable 100 MHz system clock source for the FPGA, but

which also can be clocked from external sources via the connectors. Finally, the board offers all basic functions for many FPGA applications on a tiny footprint without the need for an additional carrier board.

2. Application information

2.1. Powering the board

Be careful and make sure that the power supply is connected with the correct polarity! The ports of the screw terminal P1 are marked with + and - signs on silkscreen layer. Fig. 1 shows the right polarity.

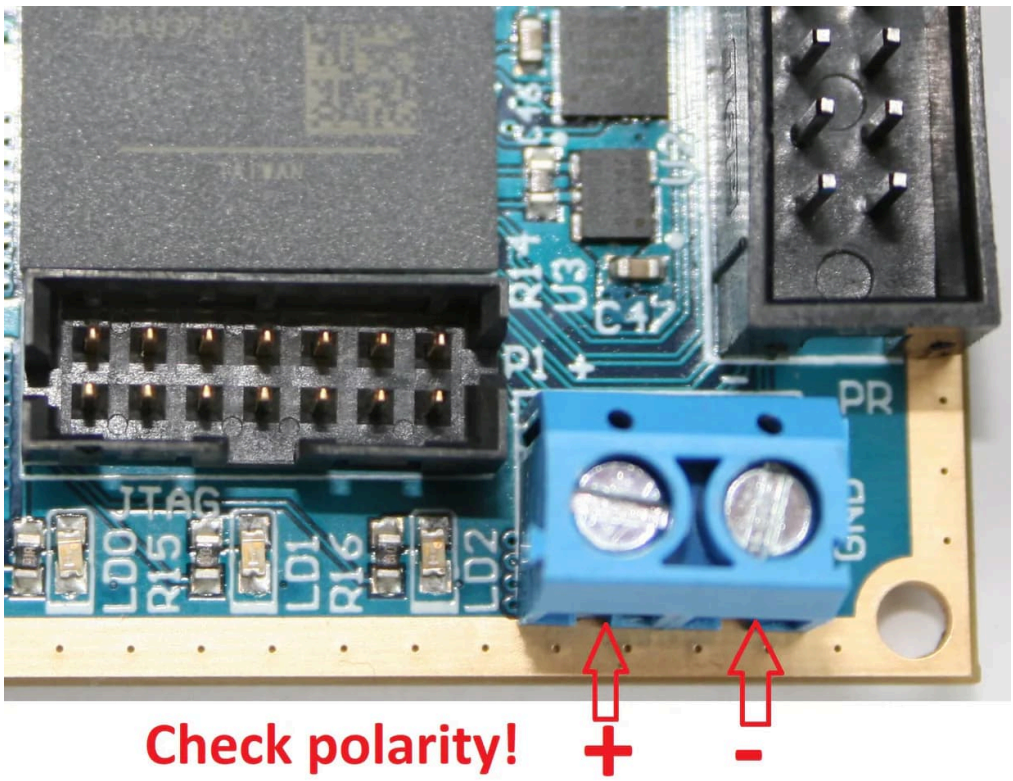


Fig. 1: Take care of the right polarity of the screw terminal power input P1. The positive terminal is located left.

Another way to power the Artix-7 FPGA Module is to use pin 1 and pin 2 of the PT header. By default, pin 1 is shorted with the positive input port (VIN) of the screw terminal, and pin 2 is shorted with GND. This configuration can be used to power the board either by the pins of the PT header or the screw terminal P1. Do not connect a voltage source to both power inputs P1 and PT header pins 1 and 2 at same time! But you can power the FPGA module via P1 (VIN and GND) and a slave module connected to the PT header pin 1 and 2(VIN and GND). Fig. 2 shows the resistors used for hardware-selectable configuration of PT and PR header. All suitable configurations are summarized in Tab. 1.

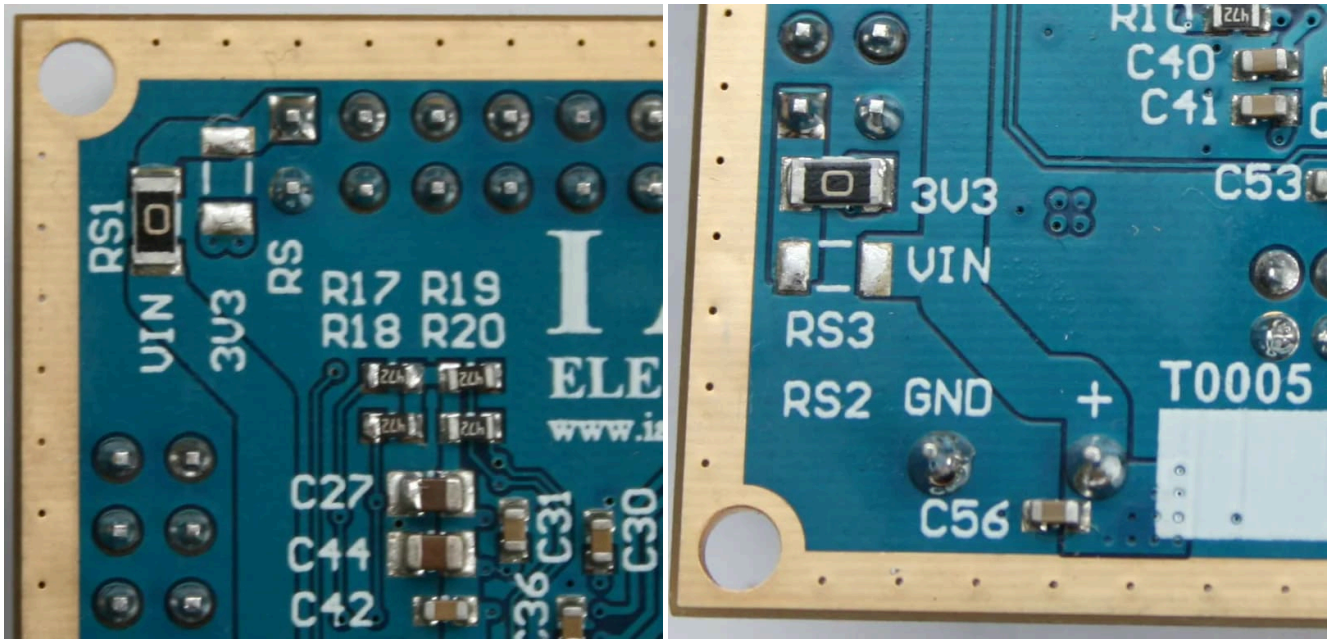


Fig. 2. Default configuration for PT header (left image): RS1 shorts VIN to pin 1. Default configuration for PR header (right image): RS3 shorts 3.3V from DC/DC switch to pin 1.

Tab. 1: Hardware-selectable voltage configuration. Pin 1 of headers PT and PR is set by resistor jumpers RS_.

	RS	RS1	RS2	RS3	PT Pin 1	PR Pin 1
1.	Open	Short (0 Ohm)	Open	Short (0 Ohm)	VIN	3.3V
2.	Open	Short (0 Ohm)	Short (0 Ohm)	Open	VIN	VIN
3.	Short (0 Ohm)	Open	Short (0 Ohm)	Open	3.3V	VIN
4.	Short (0 Ohm)	Open	Open	Short (0 Ohm)	3.3V	3.3V

Please be careful when selecting the correct input voltage configuration. The jumper resistors have case size 1206 and can be easily (de)mounted with a hot air gun.

2.2. Programming the board

Our Artix-7 FPGA Module is supported by the free edition of Xilinx Vivado (formerly WebPACK). Code can be synthesized and finally downloaded to the FPGA with the Xilinx toolchain. For this purpose, we recommend a supported programming cable like Xilinx Platform Cable USB or JTAG-HS3 Programming Cable from Digilent. Your cable must fit into the standard Xilinx JTAG header with 14 pins. Some examples are shown in Fig. 3 below.



Fig. 3: Onboard standard Xilinx JTAG header (left) with plugged Digilent JTAG-HS3 Programming Cable (middle) or Xilinx Platform Cable USB (right)

The possibilities to program the FPGA are numerous and depend on the preferences of the user. In the simplest case you use the Hardware Manager from Xilinx Vivado and program the FPGA directly with a bit-file. For a non-volatile configuration of the FPGA you have to program a valid configuration file to the onboard SPI flash. The configuration memory is an IC of S25FL064L series from Cypress Semiconductor. In the Hardware Manager from

Xilinx Vivado you have to choose the type s25fl064l-spi-x1_x2_x4 (see Fig. 4.). Please note that this device is only supported since Vivado version 2017.3.

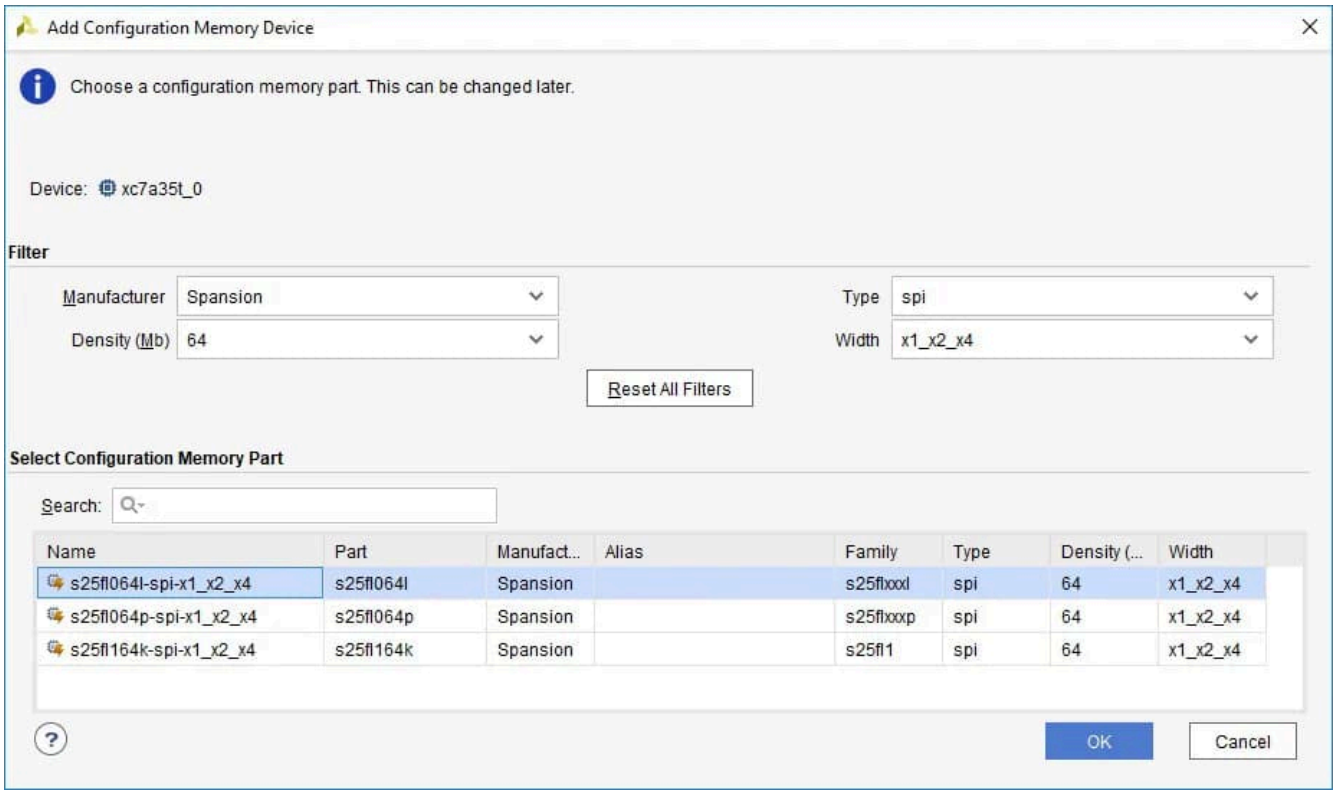


Fig. 4: Choose the right configuration memory part in Xilinx Vivado. The S25FL064L series is supported since Vivado version 2017.3.

You can check proper device functionality by reading XADC values like internal voltage levels (see Fig. 5)

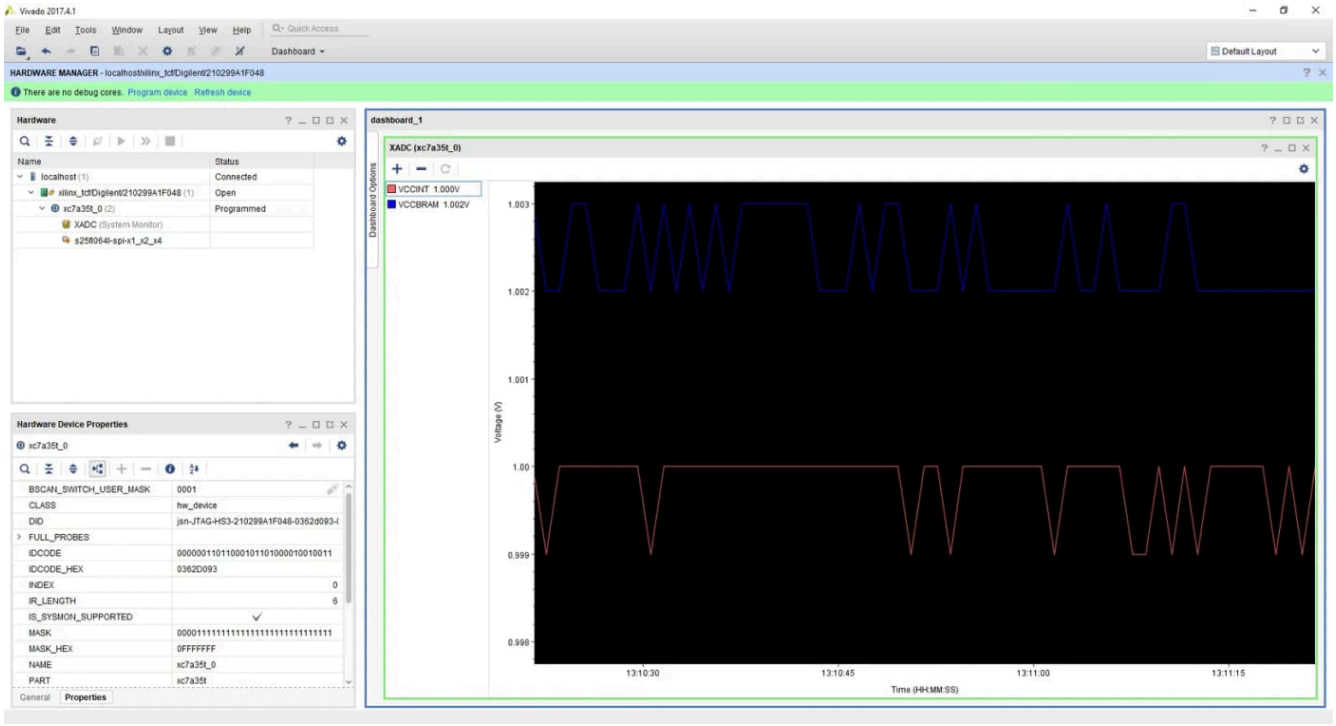


Fig. 5: Xilinx Vivado Hardware Manager can be used to read internal XADC values from the FPGA module.

With a simple test design loaded, the four user LEDs blink (fig. 6).



Fig. 6: A "hello world" test design with blinking user LEDs.

3. Electrical data (pin description)

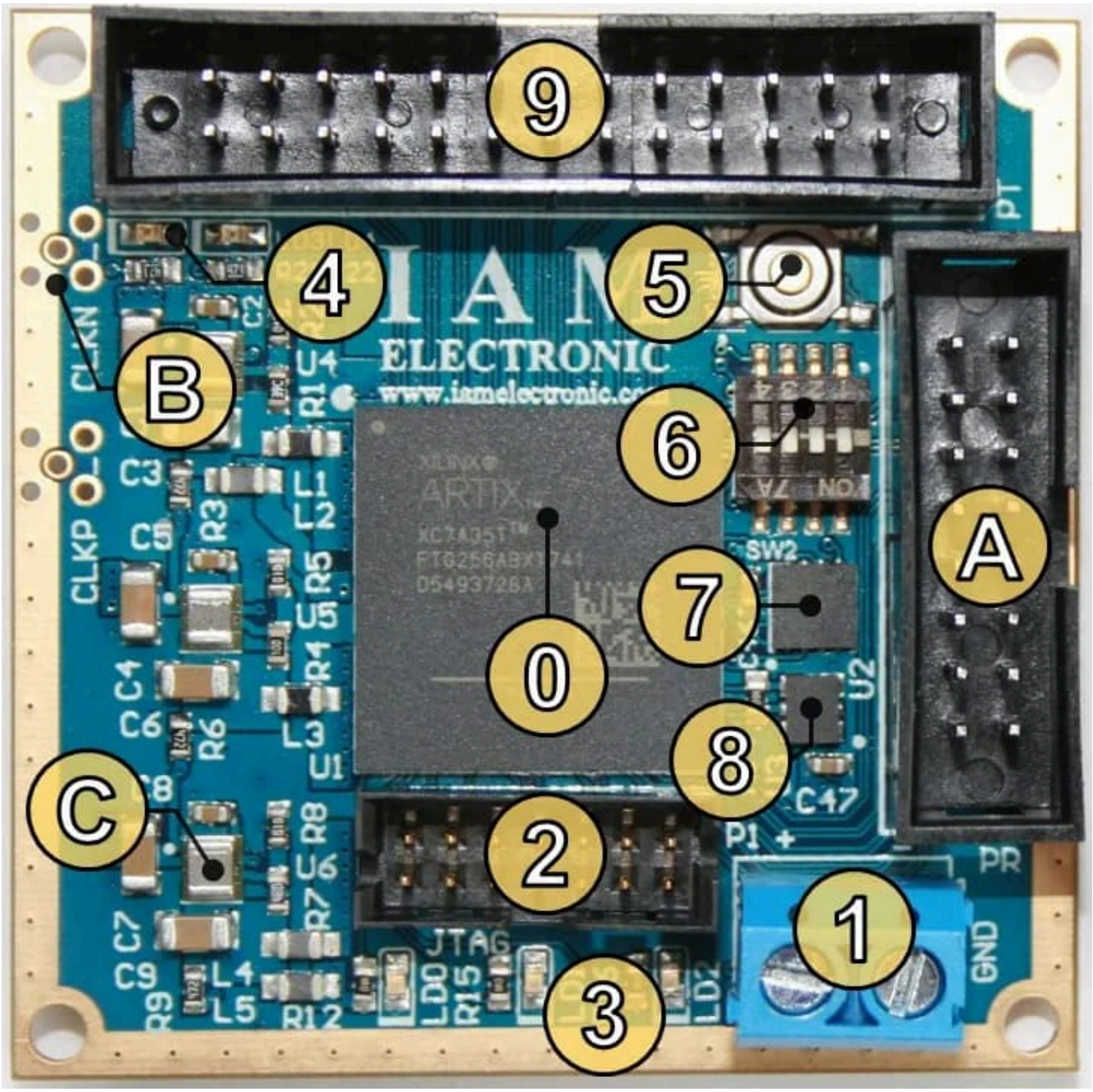


Fig. 7: An overview of all building blocks of the tiny FPGA board.

3.1 FPGA

The board is assembled with a Xilinx Artix-7 FPGA XC7A35T-1FTG256C. The speed grade of this device is -1 and operating temperature range is 0 °C to 85 °C (commercial grade). Other assemblies are available on request (see Ordering information).

3.2 P1 screw terminal

The screw terminal P1 is for direct power supply with loose cables. Recommended wire range (AWG) is 14 - 22. The wire strip length should be 5-6mm. The circuitry is designed for an input voltage of 5 V to 17 V.
Make sure the polarity is correct when connecting the cables!

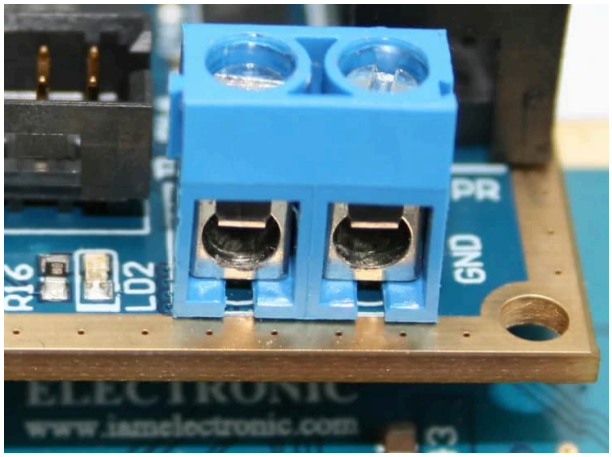


Fig. 8: Screw terminal P1 for power input (front view). Left port is positive terminal, right is negative (GND).

3.3 JTAG header

The pin assignment of the JTAG header matches the 14 pin pos. connectors of common programming cables. Some examples are shown in section 2.2. Programming the board.

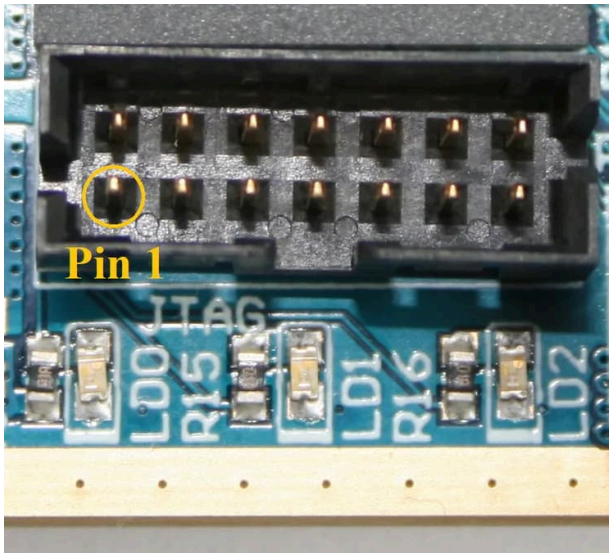


Fig. 9: Standard Xilinx JTAG Header, dual row with 14 pins (2.00 mm pitch).

Tab. 2: Electrical pinout of the JTAG header.

Board pin	Note	FPGA pin name	Bank	Location
JTAG Pin 1	GND			
JTAG Pin 2	3.3 V			
JTAG Pin 3	GND			
JTAG Pin 4	TMS	TMS_0	0	M7
JTAG Pin 5	GND			
JTAG Pin 6	TCK	TCK_0	0	L7
JTAG Pin 7	GND			
JTAG Pin 8	TDO	TDO_0	0	N8
JTAG Pin 9	GND			
JTAG Pin 10	TDI	TDI_0	0	N7
JTAG Pin 11	GND			
JTAG Pin 12	N.C			
JTAG Pin 13	GND			
JTAG Pin 14	N.C			

3.4 User LEDs (blue)

Below the JTAG connector there are three blue LEDs. They are marked with designators LD0, LD1, and LD2. LD0 indicates completion of the configuration sequence. After programming has finished, the LED will be on (until the FPGA is configured, the LED will be off). In normal operation the LED LD0 is permanently switch on. The other

two LEDs can be switched with output pins of the FPGA. The output drivers of the FPGA pins are used to power the LEDs directly. Tab. 3 shows the output pins from the FPGA connected to the LEDs.

Tab. 3: Pin assignment of User LEDs LD1 and LD2 (blue LEDs) on the FPGA.

Board pin	Note	FPGA pin name	Bank	Location
LD1 (blue LED)	High = LED on	IO_L8N_T1_34	34	T2
LD2 (blue LED)	High = LED on	IO_L8P_T1_34	34	R3

3.5 User LEDs (green and red)

In addition to the blue LEDs there is a green LED (LD3) and a red LED (LD4) on the board. Both are next to each other in the upper left corner of the board. Just like LD1 and LD2, LD3 and LD4 are driven by the output pins of the FPGA through a series resistor. The pin assignment of the green and the red LED is shown in Tab. 4.

Tab. 4: Assignment of User LEDs LD3 and LD4 (green and red LED) to the FPGA pins.

Board pin	Note	FPGA pin name	Bank	Location
LD3 (green LED)	High = LED on	IO_L5P_T0_AD13P_35	35	C7
LD4 (red LED)	High = LED on	IO_L5N_T0_AD13N_35	35	C6

3.6 Reset button

The button SW1 on top right corner of the board triggers a manual reset of the FPGA.

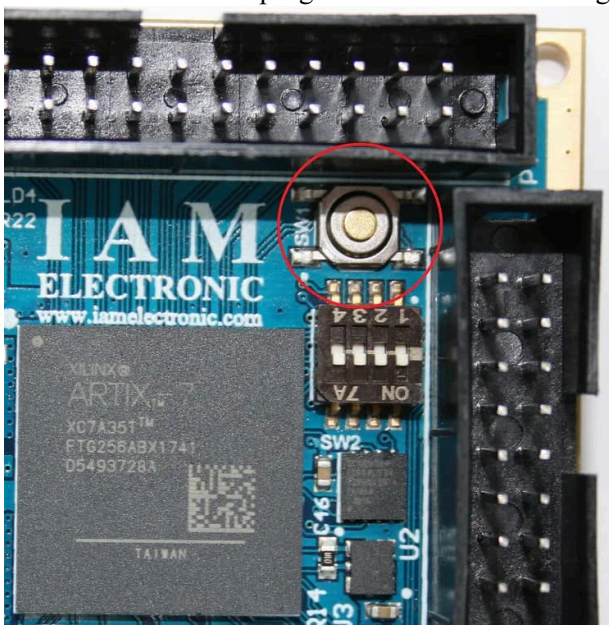


Fig. 10: Reset button SW1.

In the unpressed state the PROGRAM_B pin of the FPGA is pulled high, and while pushing the button this pin is tied to GND. On falling edge, the FPGA configuration is cleared and configuration sequence is initiated upon the following rising edge. Because the FPGA is permanently configured to Master SPI mode, a new sequence will load configuration data from SPI flash.

Tab. 5: Assignment of Reset button SW1 to the FPGA.

Board pin	Note	FPGA pin name	Bank	Location
SW1	Unpressed = High, pressed = Low	PROGRAM_B_0	0	L9

3.7 Micro switches

The four micro DIP switches SW2 can be used for user inputs.

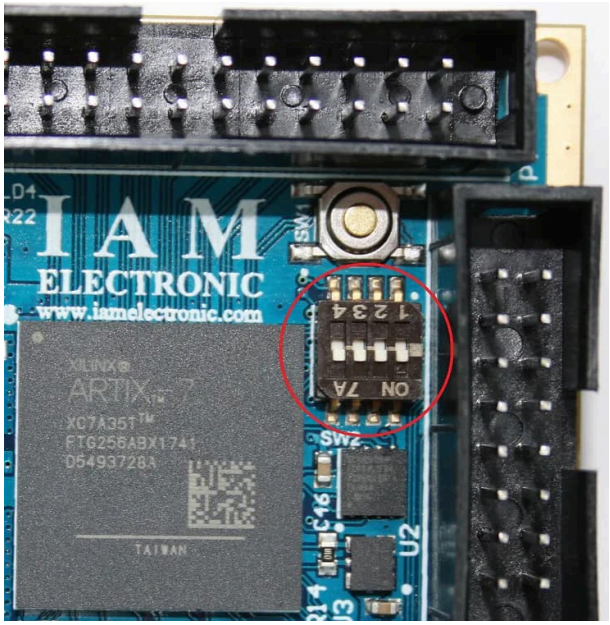


Fig. 11: Micro DIP switches SW2.

Due to the small dimensions of the switches, these can probably be used for coding fixed values or states rather than for user inputs. During OFF-state of the switches, the associated pins of the FPGA are pulled high. In ON-state, they are tied to GND. The ON position of the switches is marked on the case, and the assigned pins are shown in Tab. 6.

Tab. 6: Assignment of micro switches SW2 to the FPGA.

Board pin	Note	FPGA pin name	Bank	Location
SW2 No. 1	Off = High, On = Low	IO_L17P_T2_A26_15	15	E16
SW2 No. 2	Off = High, On = Low	IO_L17N_T2_A25_15	15	D16
SW2 No. 3	Off = High, On = Low	IO_L18P_T2_A24_15	15	F15
SW2 No. 4	Off = High, On = Low	IO_L18N_T2_A23_15	15	E15

3.8 Configuration memory (SPI flash)

The non-volatile configuration for the FPGA can only be loaded in Master SPI mode (FPGA pins M[2:0]=001) from the attached memory device U2 (SPI flash).

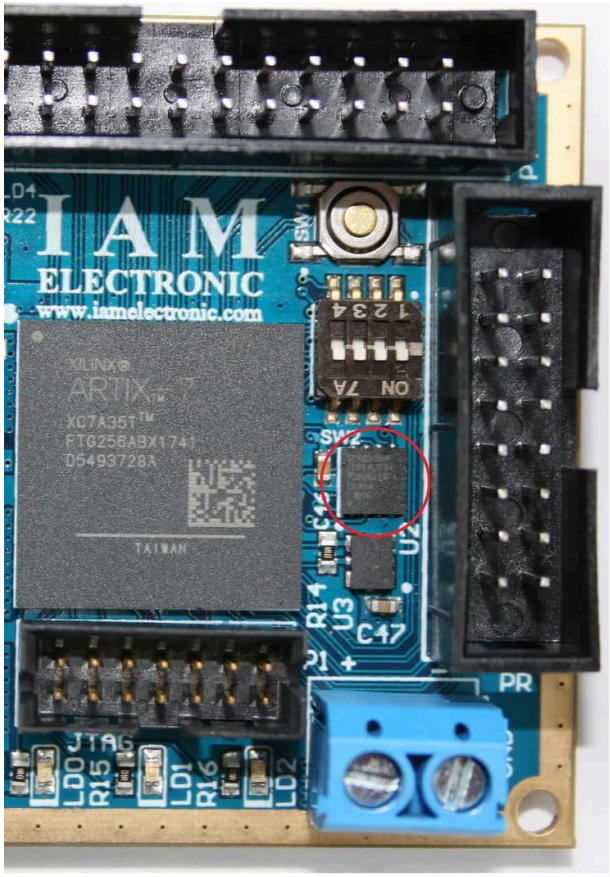


Fig. 12: 64 Mbit SPI configuration flash.

During configuration, internal pull-up resistors are disabled on each SelectIO pin, because pin L15 PUDC_B is permanently pulled high. The flash is from S25FL064L series from Cypress Semiconductor.
Since Xilinx Vivado version 2017.3 these series is supported (see Xilinx UG908, Table C-1: Supported Flash Memory Devices for Artix-7 Device Configuration). The flash memory has a density of 64 Mbit. The entire configuration bitstream length for the Xilinx XC7A35T is 17,536,096 bit (see Xilinx UG470, Table 1-1: Bitstream Length).
In Xilinx Vivado, you have to choose *s25fl064l-spi-x1_x2_x4* device for configuration memory (see section 2.2. Programming the board for details). The FPGA pins used to control the SPI flash are listed in Tab. 7

Tab. 7: Assignment of SPI flash and configuration pins to the FPGA.

Board pin	Note	FPGA pin name	Bank	Location
U2 pin 6	SCK	CCLK_0	0	E8
U2 pin 1	CS#	IO_L6P_T0_FCS_B_14	14	L12
U2 pin 5	SI/IO0	IO_L1P_T0_D00_MOSI_14	14	J13
U2 pin 2	SO/IO1	IO_L1N_T0_D01_DIN_14	14	J14
U2 pin 3	WP#/IO2	IO_L2P_T0_D02_14	14	K15
U2 pin 7	HOLD#/IO3	IO_L2N_T0_D03_14	14	K16
Pull-Up R13	High	M0_0	0	M9
GND	Low	M1_0	0	M10
GND	Low	M2_0	0	M11
Pull-Up R10	High	IO_L3P_T0_DQS_PUDC_B_14	14	L15

3.9 Clock source 100 MHz

A low-jitter precision oscillator generates a stable system clock for the FPGA. The board has a DSC1123CI5-100.000 MEMS oscillator (U3) with 100 MHz output clock frequency.

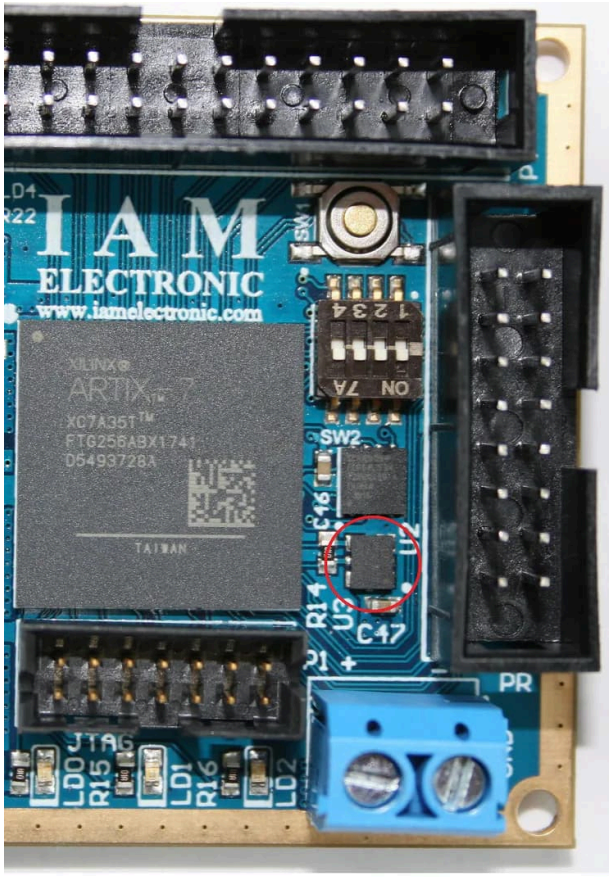


Fig. 13: 100 MHz clock source.

The operating temperature is from −40 °C to 85 °C with a frequency stability of ±10 ppm. The clock source has a LVDS output with ΔVpp of 350 mV. The output is terminated with a 100 Ω resistor (R14) on the FPGA board. The differential clock signal is routed to a Multi-region Clock Capable (MRCC) clock input on bank 14 (see Tab. 8).

Tab. 8: Assignment of differential clock signals to the FPGA pins.

Board pin	Note	FPGA pin name	Bank	Location
U3 pin 4	100 MHz Output from U3	IO_L13P_T2_MRCC_14	14	N11
U3 pin 5	100 MHz Output from U3	IO_L13N_T2_MRCC_14	14	N12

3.10 PT header (26 pos.)

The header on top of the board (PT) is a shrouded dual row 26 pin header with 2.54 mm pitch.

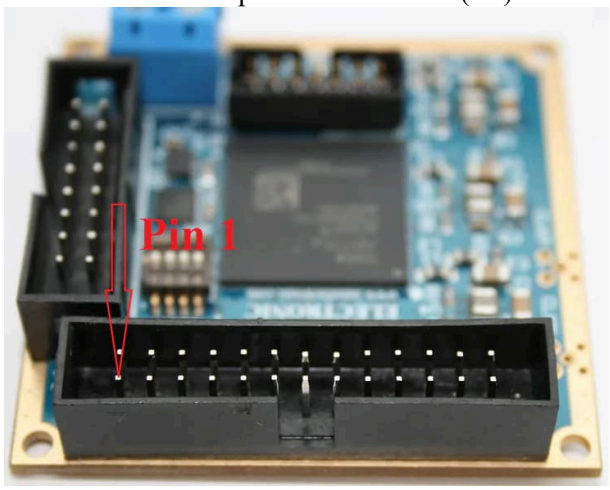


Fig. 14: PT header with 26 positions.

There are 22 general purpose input/outputs (GPIOs) and two separate power pins with corresponding GND pins. The voltage of the power pins can be hardware-selected with the resistor jumpers (0 Ω) RS and RS1 (see Tab. 1). FPGA pins with an *AD* in the designator can be used as analog inputs. For more information see Xilinx XADC documentation (Xilinx UG480).

Tab. 9: Pin mapping of header PT with corresponding FPGA pins.

Board pin	Note	FPGA pin name	Bank	Location
PT pin 1	3.3 V or VIN	-	-	-
PT pin 2	GND	-	-	-
PT pin 3		IO_L7P_T1_AD2P_15	15	A13
PT pin 4		IO_L7N_T1_AD2N_15	15	A14
PT pin 5		IO_L5N_T0_AD9N_15	15	A12
PT pin 6		IO_L5P_T0_AD9P_15	15	B12
PT pin 7		IO_L4P_T0_15	15	B10
PT pin 8		IO_L4N_T0_15	15	B11
PT pin 9		IO_L3P_T0_DQS_AD1P_15	15	B9
PT pin 10		IO_L3N_T0_DQS_AD1N_15	15	A10
PT pin 11		IO_L2P_T0_AD8P_15	15	A8
PT pin 12		IO_L2N_T0_AD8N_15	15	A9
PT pin 13		IO_L1N_T0_AD4N_35	35	A7
PT pin 14		IO_L1P_T0_AD4P_35	35	B7
PT pin 15		IO_L2N_T0_AD12N_35	35	B5
PT pin 16		IO_L2P_T0_AD12P_35	35	B6
PT pin 17		IO_L3N_T0_DQS_AD5N_35	35	A4
PT pin 18		IO_L3P_T0_DQS_AD5P_35	35	A5
PT pin 19		IO_L4N_T0_35	35	A3
PT pin 20		IO_L4P_T0_35	35	B4
PT pin 21		IO_L8P_T1_AD14P_35	35	B2
PT pin 22		IO_L8N_T1_AD14N_35	35	A2
PT pin 23	Clock capable	IO_L12N_T1_MRCC_15	15	C13
PT pin 24	Clock capable	IO_L12P_T1_MRCC_15	15	D13
PT pin 25	GND	-	-	-
PT pin 26	3.3 V	-	-	-

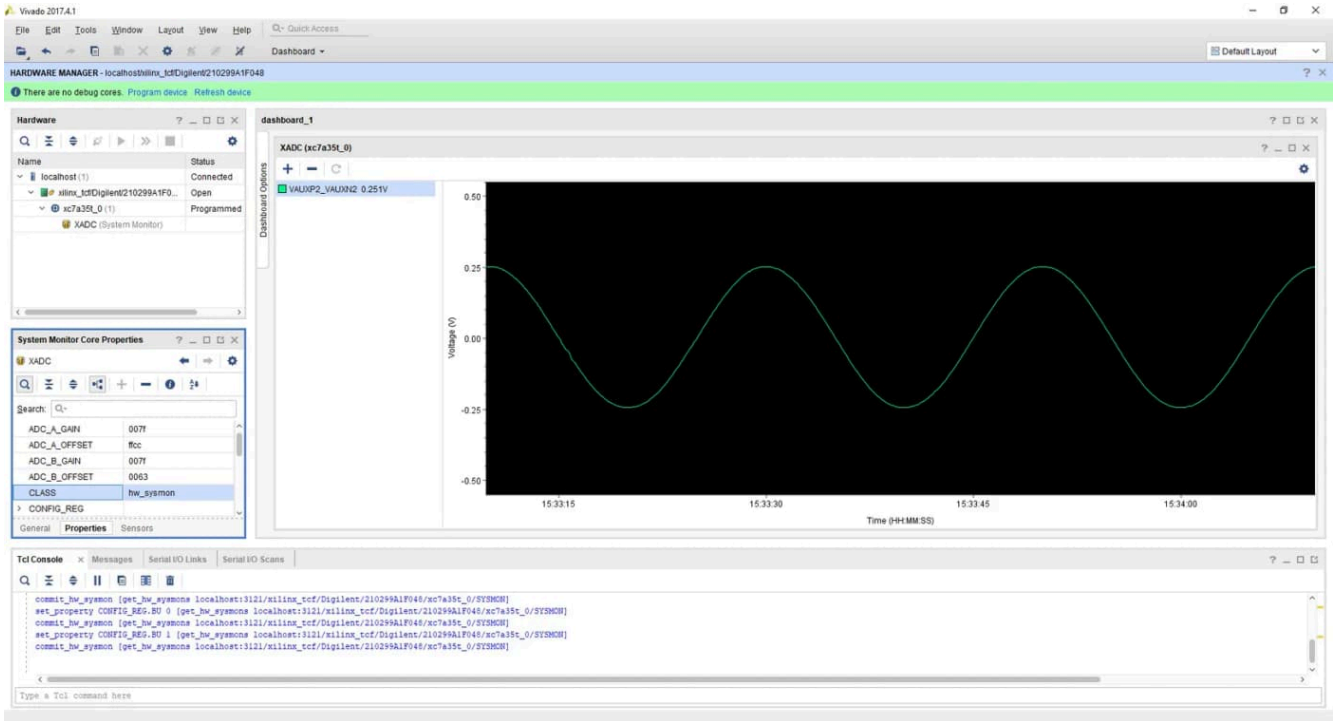


Fig. 15: Xilinx Vivado Hardware Manager can be used to visualize analog input samples.

3.11 PR header (16 pos.)

The header on the right of the board (PR) is a shrouded dual row 16 pin header with 2.54 mm pitch.

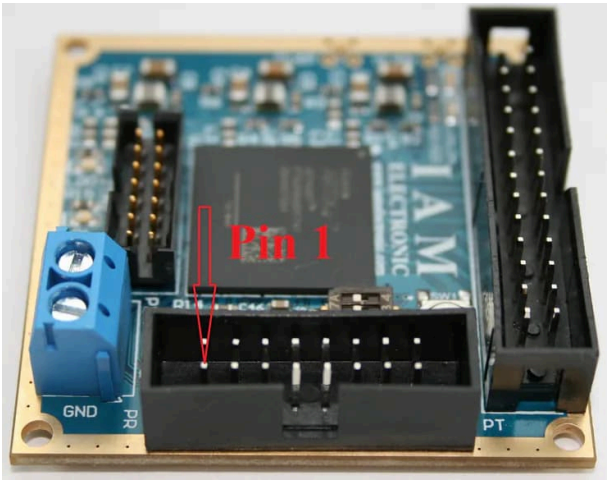


Fig. 16: PR header with 16 positions.

There are 14 general purpose input/outputs (GPIOs) and a separate power pin with corresponding GND pin. The voltage of the power pin can be hardware-selected with the resistor jumpers (0 Ω) RS2 and RS3 (see Tab. 1). FPGA pins with an *AD* in the designator can be used as analog inputs. For more information see Xilinx XADC documentation (Xilinx UG480).

Tab. 10: Pin mapping of header PR with corresponding FPGA pins.

Board pin	Note	FPGA pin name	Bank	Location
PR pin 1	3.3 V or VIN	-	-	-
PR pin 2	GND	-	-	-
PR pin 3		IO_L17N_T2_A13_D29_14	14	R11
PR pin 4		IO_L17P_T2_A14_D30_14	14	R10
PR pin 5		IO_L15P_T2_DQS_RDWR_B_14	14	R12
PR pin 6		IO_L15N_T2_DQS_DOUT_CSO_B_14	14	T12
PR pin 7		IO_L16P_T2_CSI_B_14	14	R13
PR pin 8		IO_L16N_T2_A15_D31_14	14	T13
PR pin 9		IO_L10N_T1_D15_14	14	T15
PR pin 10		IO_L10P_T1_D14_14	14	T14
PR pin 11		IO_L9N_T1_DQS_D13_14	14	R16
PR pin 12		IO_L9P_T1_DQS_14	14	R15
PR pin 13		IO_L10N_T1_AD11N_15	15	B16
PR pin 14		IO_L10P_T1_AD11P_15	15	C16
PR pin 15		IO_L9N_T1_DQS_AD3N_15	15	A15
PR pin 16		IO_L9P_T1_DQS_AD3P_15	15	B15

3.12 External clock I/O (optional MMCX jacks)

The optional MMCX jacks can be used for clock input or output signals, or even as general purpose I/Os.

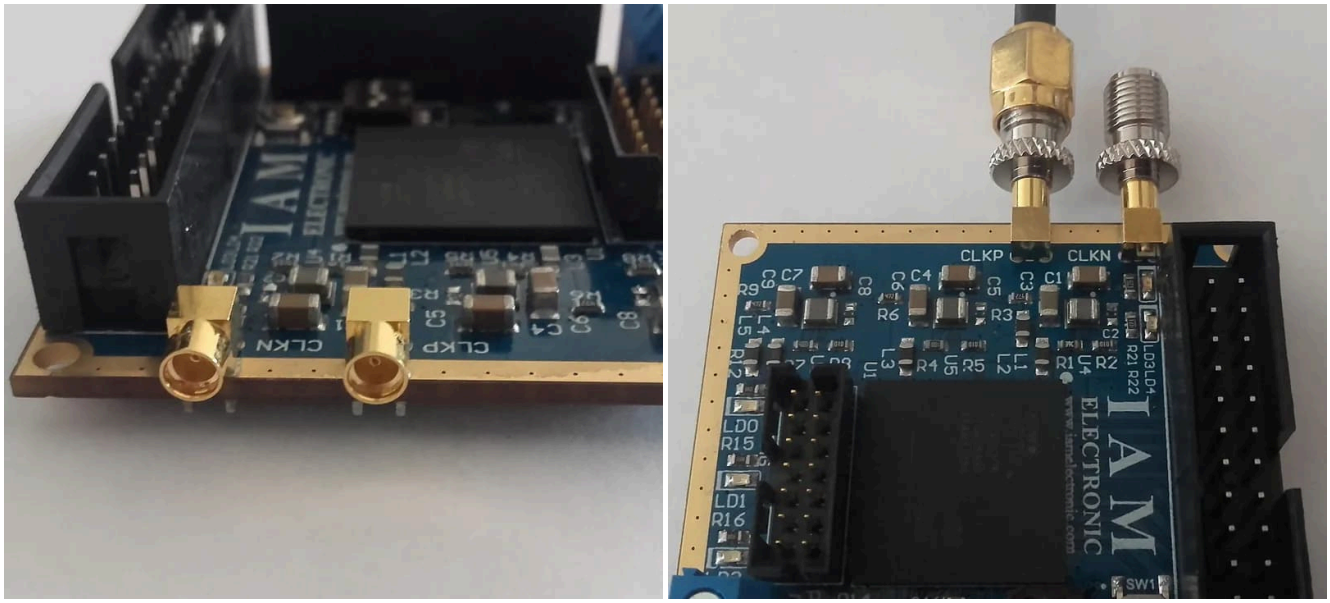


Fig. 17. Optional MMCX jacks for clock input and output signals (left picture). With an appropriate adapter, the connectors are also suitable for SMA cables (right picture).

Tab. 11: Pin assignment of the optional external MMCX clock inputs/outputs.

Board pin	Note	FPGA pin name	Bank	Location
CLK_P	Multi-region Clock Capable	IO_L12P_T1_MRCC_35	35	D4
CLK_N	Multi-region Clock Capable	IO_L12N_T1_MRCC_35	35	C4

3.13 DC/DC converter for I/O voltage

All I/O banks (bank 0, 14, 15, 34, and 35) of the FPGA are powered by 3.3 V. The voltage is provided by an onboard DC/DC converter which is capable of driving an output current of 2 A. All current sinks connected to the board and the FPGA itself must be considered to not exceed the current limit of 2 A! Further, we recommend the following constraints regarding the configuration of the FPGA:

set_property CFGBVS VCCO [current_design];
set_property CONFIG_VOLTAGE 3.3 [current_design];

For single ended IO we recommend following constraint template for IOSTANDARD of a pin:

*set_property IOSTANDARD LVCMOS33 [get_ports *];*

and for differential IO use Transition Minimized Differential Signaling (TMDS) standard:

*set_property IOSTANDARD TMDS_33 [get_ports *];*

4. Mechanical data

Following drawings show relevant mechanical dimensions of the board. All dimensions are in millimeters (mm).

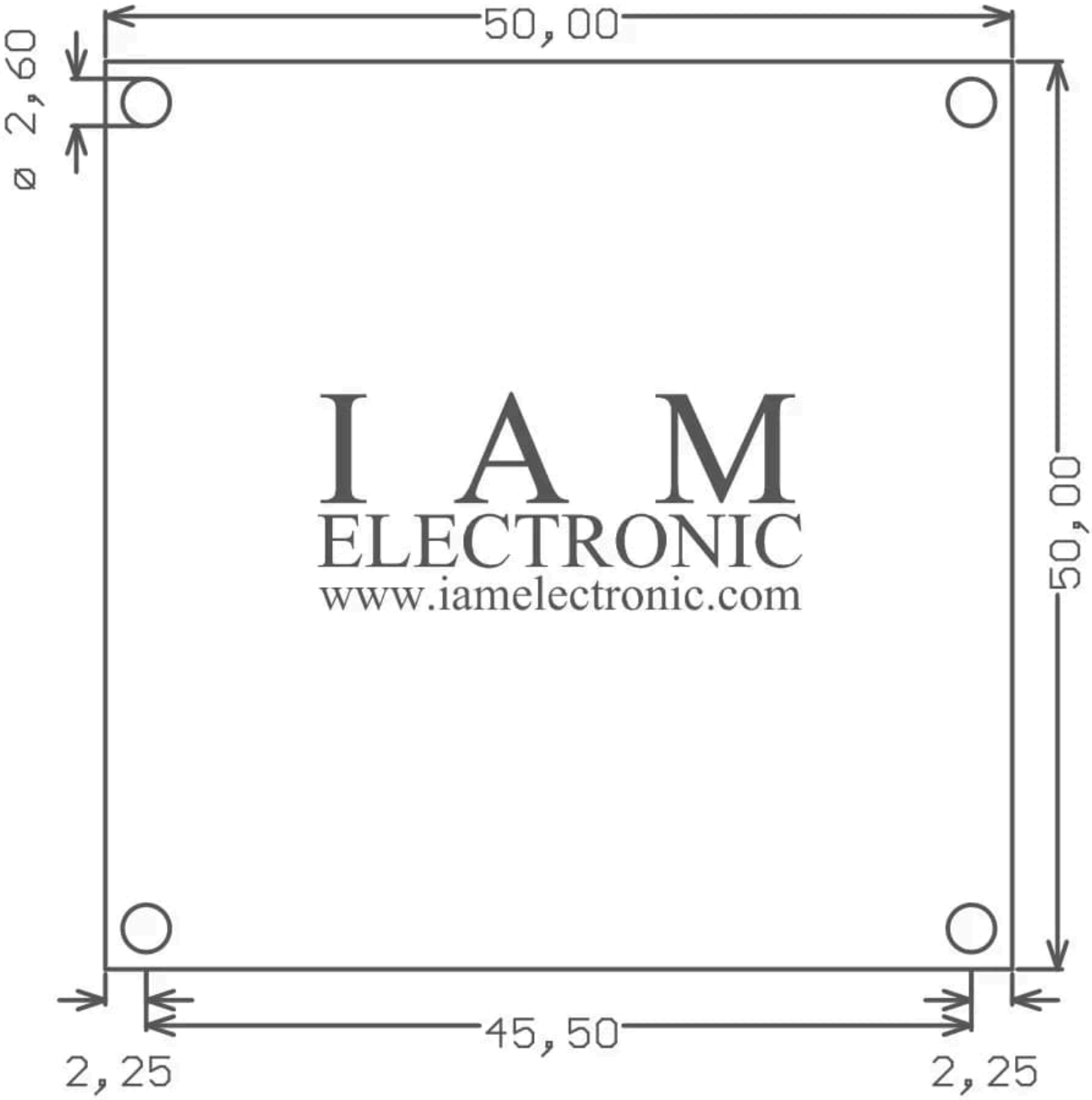


Fig. 18: Mechanical dimension of the FPGA module (board outline and mounting holes).

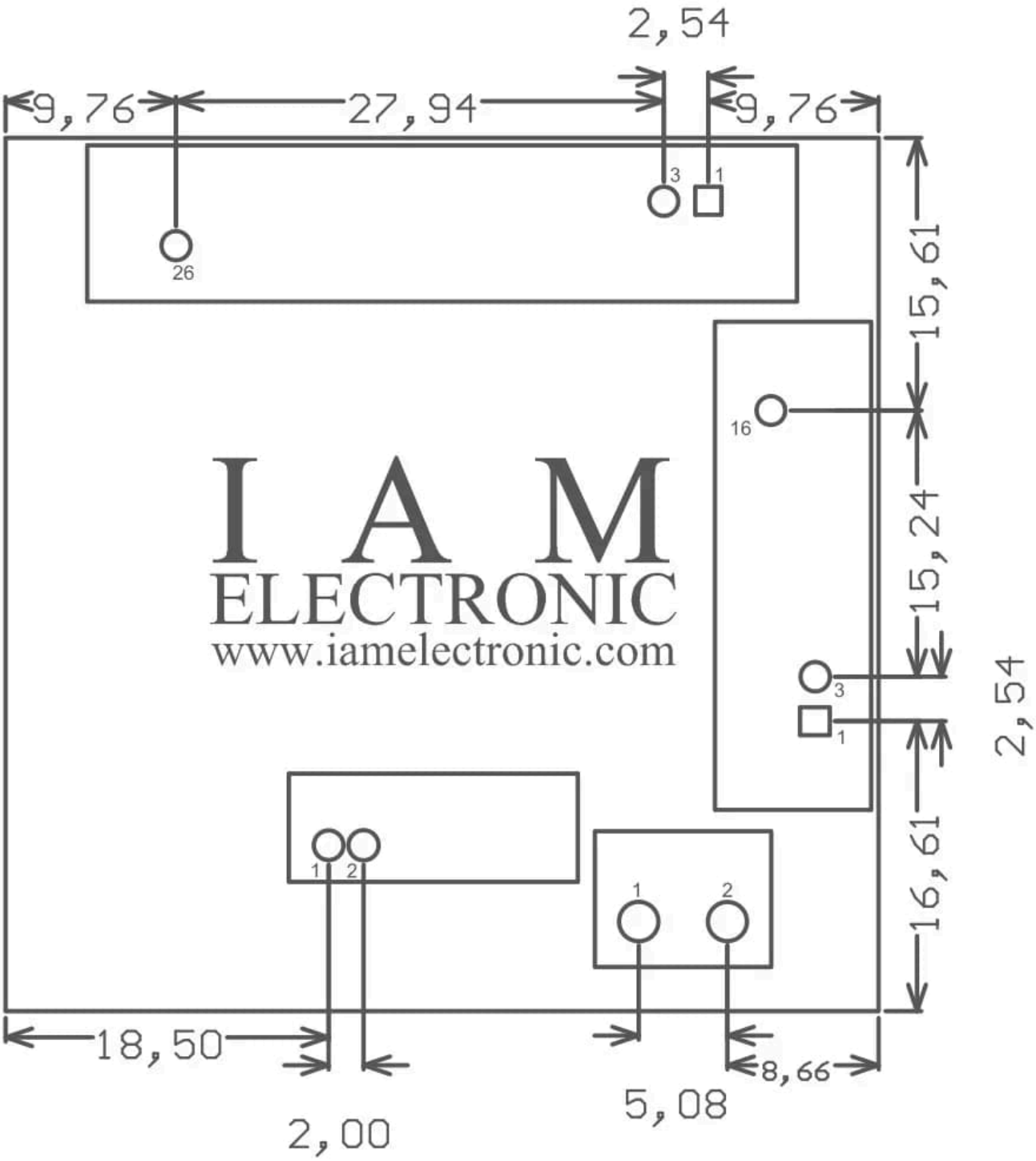


Fig. 19: Mechanical dimension of the FPGA module (connectors and pin positions).

5. Ordering information

The T0005 Artix-7 FPGA Module can be ordered at various online market places, or you can request a quotation by sending an e-mail to info@iamelectronic.com.

Tab. 12: Assembly variants of Artix-7 FPGA Module with product numbers and market places.

Product no.	Description	Market place	Request quote	Standard lead time
T0005	Artix-7 FPGA Module with XC7A35T-1FTG256C; without MMCX jacks	IAM ELECTRONIC Shop Tindie #12002	info@iamelectronic.com	Currently out of stock

6. Document history

Document number:
DS#T0005

Version history:
2026/11/27: Corrections: pin name of LD4, switch designator SW2, numbering, temperature range of the oscillator, links. Empty section removed
2018/04/17: Initial release

7. Imprint

Name and registered office of the company:
IAM Electronic GmbH
Bucksdorffstr. 43
04159 Leipzig
Germany

Contact:
Phone: +49 341 26496031
E-Mail: info@iamelectronic.com

Chief Executive Officer: Dr. Philipp Födisch

Commercial register:
Register court: Amtsgericht Leipzig
Register number: HRB 34071
Value Added Tax Identification Number: DE313797981