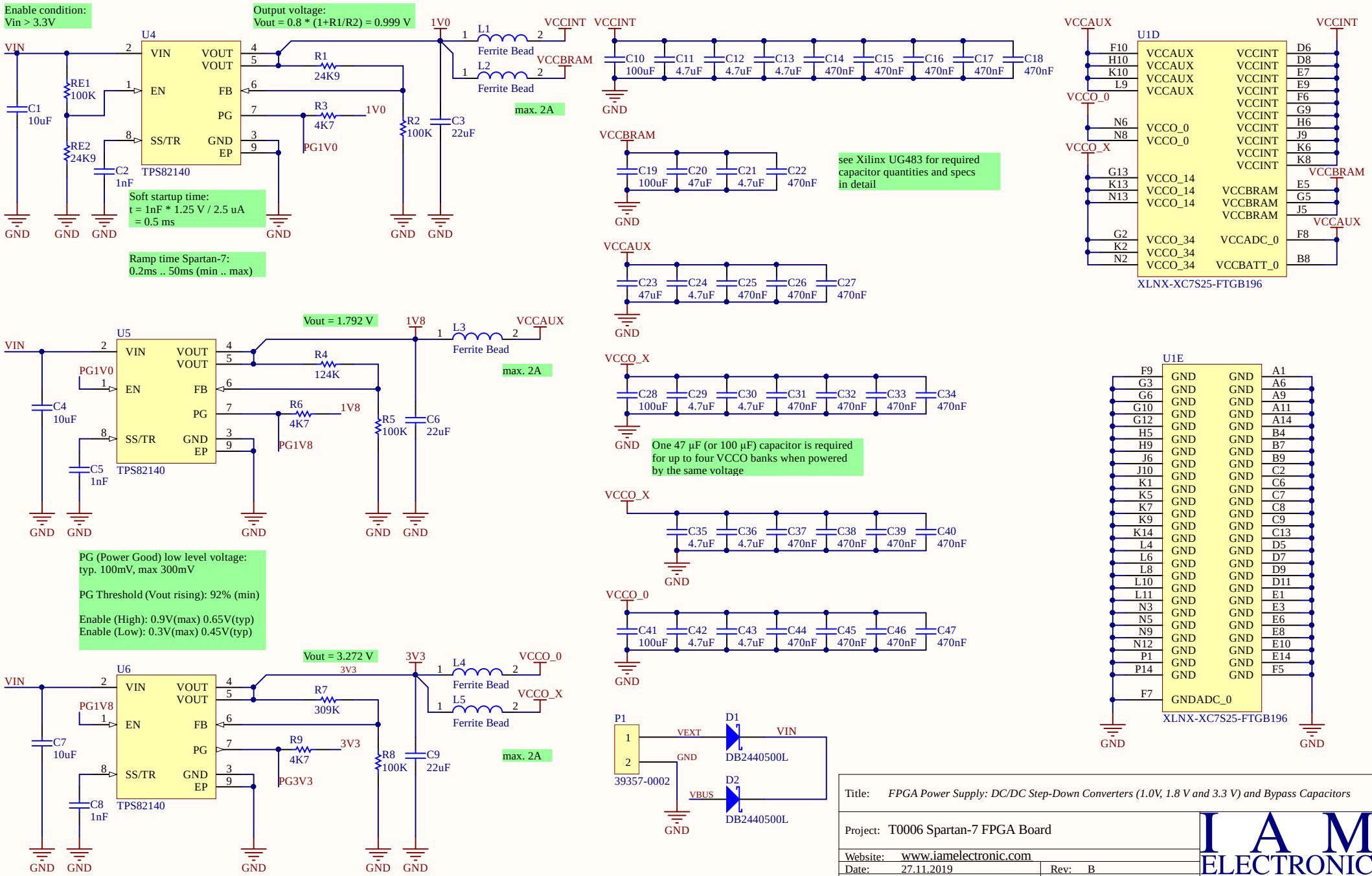
Enable condition:
Vin > 3.3V
Output voltage:
Vout = 0.8 * (1+R1/R2) = 0.999 V
U4
VIN
VOUT
EN
FB
PG
SS/TR
GND
EP
TPS82140
RE1 100K
RE2 24K9
C1 10uF
C2 1nF
R1 24K9
R2 100K
R3 4K7
C3 22uF
1V0
L1 Ferrite Bead
L2 Ferrite Bead
VCCINT
VCCBRAM
max. 2A
PG1V0
Soft startup time:
t = 1nF * 1.25 V / 2.5 uA
= 0.5 ms
Ramp time Spartan-7:
0.2ms .. 50ms (min .. max)
U5
Vout = 1.792 V
1V8
L3 Ferrite Bead
VCCAUX
R4 124K
R5 100K
R6 4K7
C4 10uF
C5 1nF
C6 22uF
PG1V8
U6
Vout = 3.272 V
3V3
L4 Ferrite Bead
L5 Ferrite Bead
VCCO_0
VCCO_X
R7 309K
R8 100K
R9 4K7
C7 10uF
C8 1nF
C9 22uF
PG3V3
PG (Power Good) low level voltage:
typ. 100mV, max 300mV
PG Threshold (Vout rising): 92% (min)
Enable (High): 0.9V(max) 0.65V(typ)
Enable (Low): 0.3V(max) 0.45V(typ)
C10 100uF
C11 4.7uF
C12 4.7uF
C13 4.7uF
C14 470nF
C15 470nF
C16 470nF
C17 470nF
C18 470nF
C19 100uF
C20 47uF
C21 4.7uF
C22 470nF
see Xilinx UG483 for required
capacitor quantities and specs
in detail
C23 47uF
C24 4.7uF
C25 470nF
C26 470nF
C27 470nF
C28 100uF
C29 4.7uF
C30 4.7uF
C31 470nF
C32 470nF
C33 470nF
C34 470nF
One 47 µF (or 100 µF) capacitor is required
for up to four VCCO banks when powered
by the same voltage
C35 4.7uF
C36 4.7uF
C37 470nF
C38 470nF
C39 470nF
C40 470nF
C41 100uF
C42 4.7uF
C43 4.7uF
C44 470nF
C45 470nF
C46 470nF
C47 470nF
P1
39357-0002
VEXT
VBUS
D1
D2
DB2440500L
U1D
XLNX-XC7S25-FTGB196
VCCAUX
VCCO_0
VCCO_X
VCCADC_0
VCCBATT_0
U1E
GNDADC_0
Title: FPGA Power Supply: DC/DC Step-Down Converters (1.0V, 1.8 V and 3.3 V) and Bypass Capacitors
Project: T0006 Spartan-7 FPGA Board
Website: www.iamelectronic.com
Date: 27.11.2019
Engineer: PFH
Rev: B
Sheet: 1 / 3
I A M
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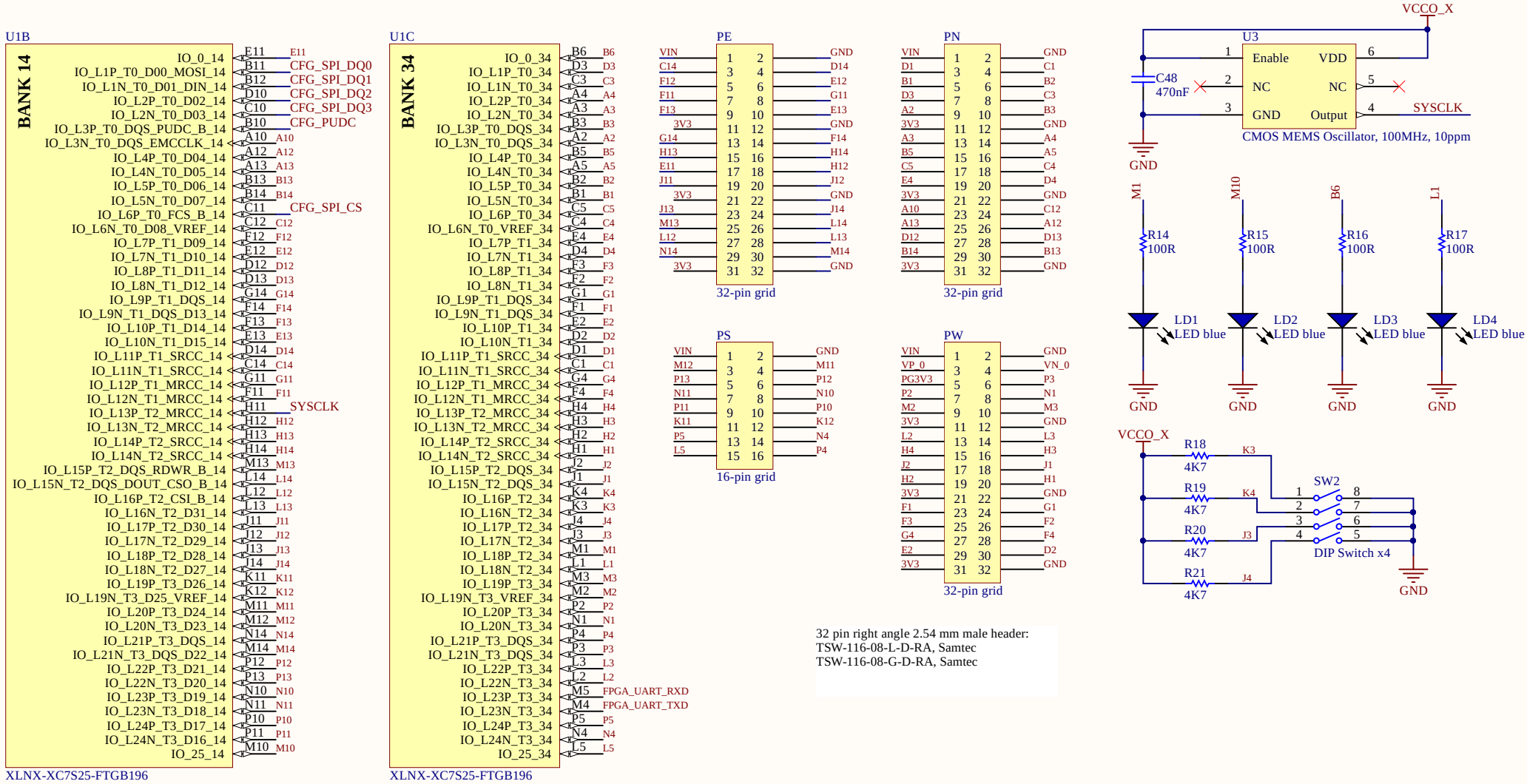
U1B
BANK 14
IO_0_14 E11 E11
IO_L1P_T0_D00_MOSI_14 B11 CFG_SPI_DQ0
IO_L1N_T0_D01_DIN_14 B12 CFG_SPI_DQ1
IO_L2P_T0_D02_14 D10 CFG_SPI_DQ2
IO_L2N_T0_D03_14 C10 CFG_SPI_DQ3
IO_L3P_T0_DQS_PUDC_B_14 B10 CFG_PUDC
IO_L3N_T0_DQS_EMCCLK_14 A10 A10
IO_L4P_T0_D04_14 A12 A12
IO_L4N_T0_D05_14 A13 A13
IO_L5P_T0_D06_14 B13 B13
IO_L5N_T0_D07_14 B14 B14
IO_L6P_T0_FCS_B_14 C11 CFG_SPI_CS
IO_L6N_T0_D08_VREF_14 C12 C12
IO_L7P_T1_D09_14 F12 F12
IO_L7N_T1_D10_14 E12 E12
IO_L8P_T1_D11_14 D12 D12
IO_L8N_T1_D12_14 D13 D13
IO_L9P_T1_DQS_14 G14 G14
IO_L9N_T1_DQS_D13_14 F14 F14
IO_L10P_T1_D14_14 F13 F13
IO_L10N_T1_D15_14 E13 E13
IO_L11P_T1_SRCC_14 D14 D14
IO_L11N_T1_SRCC_14 C14 C14
IO_L12P_T1_MRCC_14 G11 G11
IO_L12N_T1_MRCC_14 F11 F11
IO_L13P_T2_MRCC_14 H11 SYSCLK
IO_L13N_T2_MRCC_14 H12 H12
IO_L14P_T2_SRCC_14 H13 H13
IO_L14N_T2_SRCC_14 H14 H14
IO_L15P_T2_DQS_RDWR_B_14 M13 M13
IO_L15N_T2_DQS_DOUT_CSO_B_14 L14 L14
IO_L16P_T2_CSI_B_14 L12 L12
IO_L16N_T2_D31_14 L13 L13
IO_L17P_T2_D30_14 J11 J11
IO_L17N_T2_D29_14 J12 J12
IO_L18P_T2_D28_14 J13 J13
IO_L18N_T2_D27_14 J14 J14
IO_L19P_T3_D26_14 K11 K11
IO_L19N_T3_D25_VREF_14 K12 K12
IO_L20P_T3_D24_14 M11 M11
IO_L20N_T3_D23_14 M12 M12
IO_L21P_T3_DQS_14 N14 N14
IO_L21N_T3_DQS_D22_14 M14 M14
IO_L22P_T3_D21_14 P12 P12
IO_L22N_T3_D20_14 P13 P13
IO_L23P_T3_D19_14 N10 N10
IO_L23N_T3_D18_14 N11 N11
IO_L24P_T3_D17_14 P10 P10
IO_L24N_T3_D16_14 P11 P11
IO_25_14 M10 M10
XLNX-XC7S25-FTGB196
U1C
BANK 34
IO_0_34 B6 B6
IO_L1P_T0_34 D3 D3
IO_L1N_T0_34 C3 C3
IO_L2P_T0_34 A4 A4
IO_L2N_T0_34 A3 A3
IO_L3P_T0_DQS_34 B3 B3
IO_L3N_T0_DQS_34 A2 A2
IO_L4P_T0_34 B5 B5
IO_L4N_T0_34 A5 A5
IO_L5P_T0_34 B2 B2
IO_L5N_T0_34 B1 B1
IO_L6P_T0_34 C5 C5
IO_L6N_T0_VREF_34 C4 C4
IO_L7P_T1_34 E4 E4
IO_L7N_T1_34 D4 D4
IO_L8P_T1_34 F3 F3
IO_L8N_T1_34 F2 F2
IO_L9P_T1_DQS_34 G1 G1
IO_L9N_T1_DQS_34 F1 F1
IO_L10P_T1_34 E2 E2
IO_L10N_T1_34 D2 D2
IO_L11P_T1_SRCC_34 D1 D1
IO_L11N_T1_SRCC_34 C1 C1
IO_L12P_T1_MRCC_34 G4 G4
IO_L12N_T1_MRCC_34 F4 F4
IO_L13P_T2_MRCC_34 H4 H4
IO_L13N_T2_MRCC_34 H3 H3
IO_L14P_T2_SRCC_34 H2 H2
IO_L14N_T2_SRCC_34 H1 H1
IO_L15P_T2_DQS_34 J2 J2
IO_L15N_T2_DQS_34 J1 J1
IO_L16P_T2_34 K4 K4
IO_L16N_T2_34 K3 K3
IO_L17P_T2_34 J4 J4
IO_L17N_T2_34 J3 J3
IO_L18P_T2_34 M1 M1
IO_L18N_T2_34 L1 L1
IO_L19P_T3_34 M3 M3
IO_L19N_T3_VREF_34 M2 M2
IO_L20P_T3_34 P2 P2
IO_L20N_T3_34 N1 N1
IO_L21P_T3_DQS_34 P4 P4
IO_L21N_T3_DQS_34 P3 P3
IO_L22P_T3_34 L3 L3
IO_L22N_T3_34 L2 L2
IO_L23P_T3_34 M5 FPGA_UART_RXD
IO_L23N_T3_34 M4 FPGA_UART_TXD
IO_L24P_T3_34 P5 P5
IO_L24N_T3_34 N4 N4
IO_25_34 L5 L5
XLNX-XC7S25-FTGB196
PE
VIN 1 2 GND
C14 3 4 D14
F12 5 6 E12
F11 7 8 G11
F13 9 10 E13
3V3 11 12 GND
G14 13 14 F14
H13 15 16 H14
E11 17 18 H12
J11 19 20 J12
3V3 21 22 GND
J13 23 24 J14
M13 25 26 L14
L12 27 28 L13
N14 29 30 M14
3V3 31 32 GND
32-pin grid
PN
VIN 1 2 GND
D1 3 4 C1
B1 5 6 B2
D3 7 8 C3
A2 9 10 B3
3V3 11 12 GND
A3 13 14 A4
B5 15 16 A5
C5 17 18 C4
E4 19 20 D4
3V3 21 22 GND
A10 23 24 C12
A13 25 26 A12
D12 27 28 D13
B14 29 30 B13
3V3 31 32 GND
32-pin grid
PS
VIN 1 2 GND
M12 3 4 M11
P13 5 6 P12
N11 7 8 N10
P11 9 10 P10
K11 11 12 K12
P5 13 14 N4
L5 15 16 P4
16-pin grid
PW
VIN 1 2 GND
VP_0 3 4 VN_0
PG3V3 5 6 P3
P2 7 8 N1
M2 9 10 M3
3V3 11 12 GND
L2 13 14 L3
H4 15 16 H3
J2 17 18 J1
H2 19 20 H1
3V3 21 22 GND
F1 23 24 G1
F3 25 26 F2
G4 27 28 F4
E2 29 30 D2
3V3 31 32 GND
32-pin grid
32 pin right angle 2.54 mm male header:
TSW-116-08-L-D-RA, Samtec
TSW-116-08-G-D-RA, Samtec
VCCO_X
U3
Enable VDD
NC NC
GND Output
SYSCLK
C48
470nF
CMOS MEMS Oscillator, 100MHz, 10ppm
GND
M1
M10
B6
L1
R14 100R
R15 100R
R16 100R
R17 100R
LD1 LED blue
LD2 LED blue
LD3 LED blue
LD4 LED blue
VCCO_X
R18 4K7
R19 4K7
R20 4K7
R21 4K7
K3
K4
J3
J4
SW2
DIP Switch x4
Title: 82 Input/Output, System Clock (100 MHz), 4x User Switches, 4x User LEDs
Project: T0006 Spartan-7 FPGA Board
Website: www.iamelectronic.com
Date: 27.11.2019
Engineer: PFH
Rev: B
Sheet: 2 / 3
I A M
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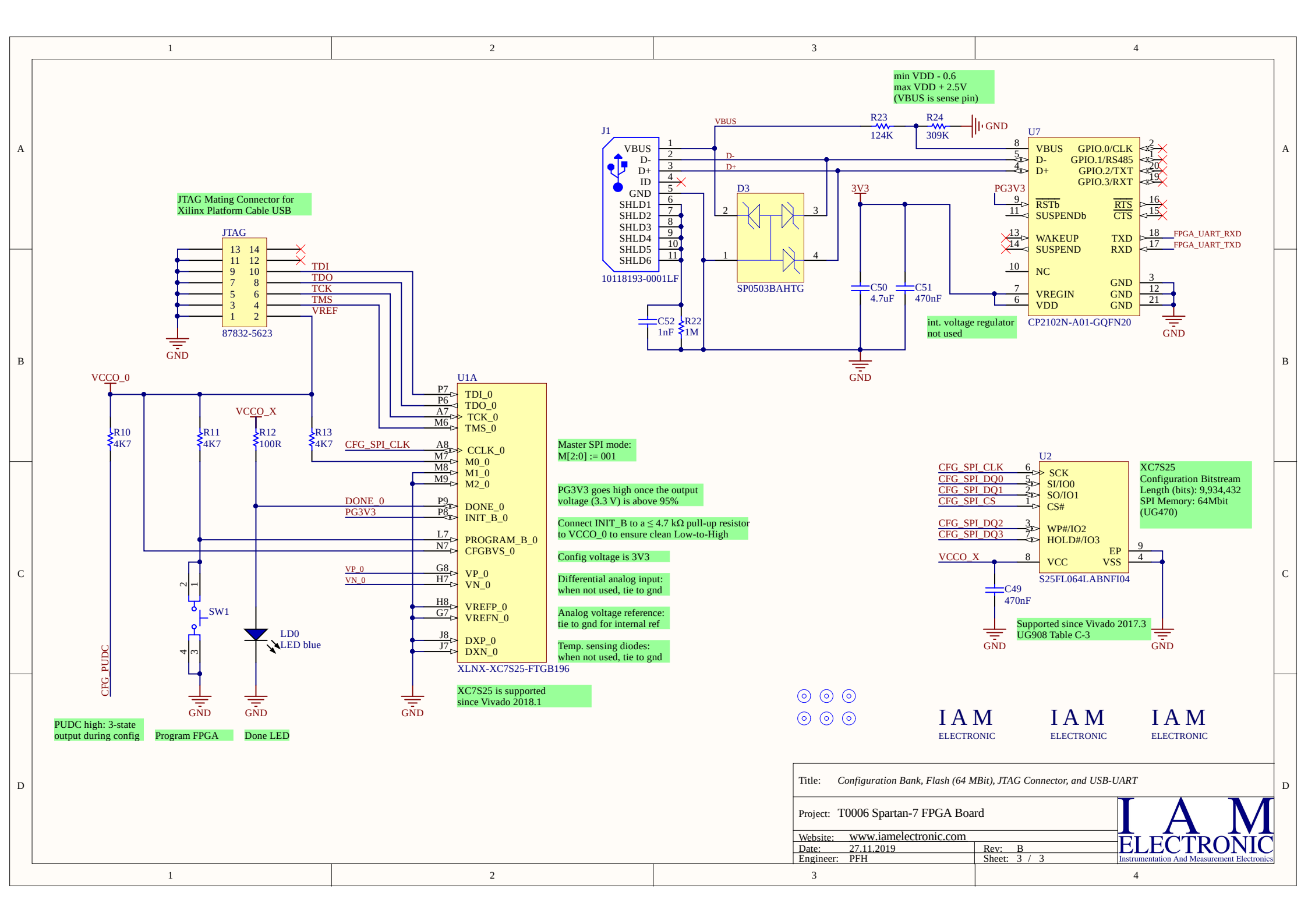

Title:	*Configuration Bank, Flash (64 MBit), JTAG Connector, and USB-UART*
Project:	T0006 Spartan-7 FPGA Board
Website:	www.iamelectronic.com
Date:	27.11.2019
Engineer:	PFH
Rev:	B
Sheet:	3 / 3

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